



**Switchmode Buck Power Converter Using Current-Mode Control<sup>®</sup>**  
*A SunCam online continuing education course*

# **Switchmode Buck Power Converter Using Current-Mode Control<sup>®</sup>**

By

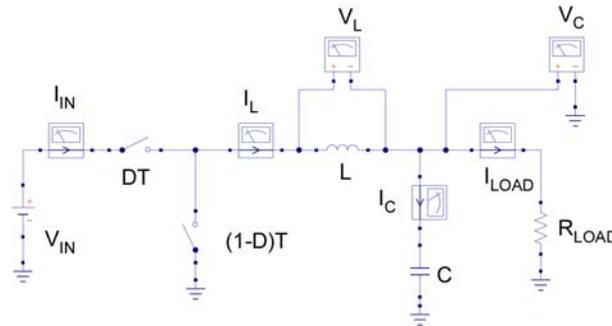
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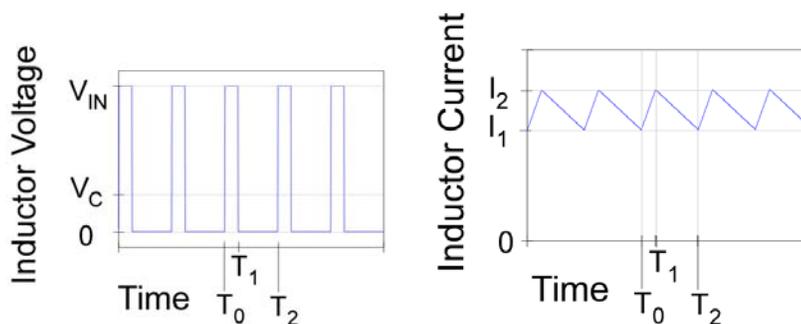
1.0 Switchmode Buck Power Converter Introduction and Basic Model

This course develops several models of the Buck converter with current-mode control. Basic operation, a practical set of examples, and large/small signal models are discussed. The considerations for feedback regulation and load-current limiting control of the converter are introduced.



**Figure 1.0 Ideal Buck converter schematic**

We employ a constant frequency, continuous current Buck converter design, with the switching period defined below in figure 1.1 by  $T_2 - T_0 = T$ . The converter initially has two conducting states defined by periods  $T_1 - T_0 = DT$  and  $T_2 - T_1 = (1 - D)T$ , corresponding to the two switching states. The  $V_{IN}$  supply is connected with the duty cycle  $D$ , and a complement controlled synchronous switch is applied to the complete the connection during the remaining  $(1 - D)$  portion of the period.



**Figure 1.1 Buck converter Inductor operating waveforms**

The inductor cannot support a DC voltage difference across its terminals. Instead, any short-term  $V_L$  voltage difference results in a rate of change of current  $I_L$  through the inductor. With some  $V_C$  voltage on the capacitor, the inductor has a voltage difference



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$V_{IN} - V_C$  applied during the  $DT$  interval and  $-V_C$  applied during the  $(I - D)T$  interval. We equate the volt-second products and keep a zero voltage average as:

$$(V_{IN} - V_C)DT - V_C(1 - D)T = 0 \quad [1.0]$$

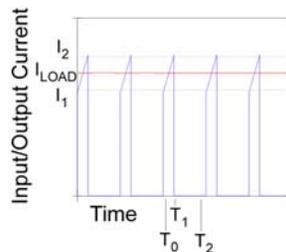
$$V_C = DV_{IN} \quad [1.1]$$

Equation [1.1] illustrates the property of the Buck converter indicating that a lower output voltage  $V_C$  can be obtained from the input  $V_{IN}$  voltage by controlling the duty cycle  $D$ . In current-mode control, feedback is separated into an inner current-control loop and an outer voltage-feedback loop. The duty-cycle  $D$  is included as an implicit result of the current control and intentionally eliminated as an explicit control variable.

## 2.0 Switchmode Buck Power Converter Input/Output Current Waveforms

As shown in figure 2.0 below, the  $I_{IN}$  input current is discontinuous and exists for the  $DT$  intervals similar to the time between  $T_1 - T_0 = DT$ . During the  $T_2 - T_1 = (I - D)T$  and similar intervals the inductor current flows in the  $(I - D)T$  controlled grounding switch element, rather than the input switch. During these periods, the input current is considered to be zero in the ideal schematic and all inductor current flows to ground, but may consist of leakage, and transient waveforms in a practical input circuit.

The  $I_{LOAD}$  output current, however, is continuous and flows through the  $R_{LOAD}$  resistor as a combination of currents from the inductor and the capacitor. Because the capacitor cannot support a continuous current, but does sink/source AC and transient currents, the average current to the load is identical to the average  $I_L$  inductor current.



**Figure 2.0 Buck converter Input and Output Current waveforms**

The average input current during the  $T_1 - T_0 = DT$  interval is identical to the  $I_{LOAD}$  output current, but because it is non-zero only during that interval, its average value is  $DI_{LOAD}$  over the entire period.



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### 3.0 Switchmode Buck Power Converter Input/Output Power and Efficiency

We can calculate the average input power from the product of the input  $V_{IN}$  supply times the average  $DI_{LOAD}$  input current as follows:

$$P_{IN} = V_{IN} \bullet DI_{LOAD} \quad [3.0]$$

Similarly, we can calculate the average output power from the product of the output  $V_C$  output times the average  $I_{LOAD}$  output current as follows:

$$P_{OUT} = V_C \bullet I_{LOAD} \quad [3.1]$$

If we insert equation [1.1] for the value of  $V_C$  in terms of the  $V_{IN}$  input voltage, we find that the input and output average power levels are identical and imply 100% efficiency:

$$P_{OUT} = DV_{IN} \bullet I_{LOAD} = P_{IN} \quad [3.2]$$

This indicated 100% efficiency is not achievable in practice because there are losses in the switching elements and the non-ideal practical components that we must use to implement the design, but high efficiencies are achievable, often exceeding 90% in practical designs. The high efficiency of the switch-mode power converters explains the interest, despite complexities of the controller required to implement practical designs.

### 4.0 Output Load Current Range

The worst-case load consideration is determined by the range of  $R_{LOAD}$  resistor values and associated with the smallest  $R_{LOAD}$  value, which in turn causes the highest  $I_{LOAD}$  value. The current handling capacity of the switching devices must be sufficient to support switching the maximum  $I_{LOAD}$  value with sufficient speed to support both  $DT$  and  $(1 - D)T$  periods. Current-mode control facilitates a means for establishing an output current limit in the operation of the Buck converter.

The maximum value of the  $R_{LOAD}$  resistor may be constrained to determine a minimum  $I_{LOAD}$  value to ensure continuous load current, to ensure stability requirements. Current-mode control permits a smooth transition to a discontinuous current operation with an additional conduction state that is not considered here.

### 5.0 Input/Output Ripple Current Effects in Ideal Component Value Selection

We see from equation [1.1] that the frequency does not enter directly into the relationship between the input voltage and the output voltage, only the duty cycle  $D$  is directly



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involved. In figure 1.1, we also see that the continuous inductor current forms a triangular waveform between the  $I_2$  peak current, and the  $I_1$  valley current.

From the fundamental differential equation description of the behavior of an ideal inductor we have:

$$V_L = L \bullet \frac{dI_L}{dt} \quad [5.0]$$

For a regime with relatively short times, relatively large inductor values, and relatively small voltages, we can approximate the relationship with line segments as follows:

$$V_L = L \bullet \frac{\Delta I_L}{\Delta t} \quad [5.1]$$

And in more useful form:

$$\Delta I_L = I_2 - I_1 = \frac{V_L \bullet \Delta t}{L} \quad [5.2]$$

From equation [5.2], we see that the “volt\*second product” of the applied waveform is used to determine the triangular “ripple” current between the  $I_2$  and  $I_1$  limits. To ensure continuous operation, we implement the design so that  $I_1$  remains non-zero by selecting an inductor value large enough to support the “volt\*second product” implied by the remaining design parameters.

Also implicit in equation [5.3] and the ripple current is a boundary condition on the capacitor value. From the fundamental differential equation description of the behavior of an ideal capacitor we have:

$$I_C = C \bullet \frac{dV_C}{dt} \quad [5.3]$$

And in more useful form:

$$\Delta V_C = \frac{I_{C-Pk-to-Pk}}{C} \Delta t = \frac{I_2 - I_1}{C} \Delta t \quad [5.4]$$

Equation [5.4] offers a value for the peak-to-peak ripple voltage that can be expected to be caused by the choice of capacitor value, time intervals, and ripple currents.



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With current-mode control, the inductor current is measured and controlled and as a consequence the ripple current is typically chosen to be a large percentage of the highest average current supplied to provide a reasonable control signal.

Non-ideal behaviors describe the power losses of inductor and capacitor parasitic loss component terms. The DC resistance of the inductor can also be used to develop a signal that is proportional to the inductor current. There is a trade-off between providing a large signal with higher losses by using a large resistance versus developing a smaller signal with smaller losses by using a smaller resistance.

### **6.0 Input/Output Voltage Range Considerations**

Practical applications require that we provide a controlled value for  $V_C$  over a range of input voltage  $V_{IN}$  values.

Automotive applications may require a nominal 12V  $V_{IN}$  operation, but be expected to function nominally under a low battery condition below 10V, and also operate with transient  $V_{IN}$  values in excess of 52V for a few milliseconds in the case of “load-dump” of highly inductive DC motor and solenoid devices connected to that same battery/alternator system. The  $V_{IN}$  range can be >5:1 for some automotive applications.

Similarly, it is common to provide “line-powered” applications that are expected to function correctly without switching circuitry when powered from 110/220V mains sources. The line-powered ranges may be ~85V from the low-line 110V source, but also higher than 365V under high-line 220V sourcing. The  $V_{IN}$  range can be >4.5:1 for some “line-powered” applications.

Although many applications require a fixed output voltage, there are also applications that require a user-programmed output voltage, often over a considerable range of values.

The capacitor must withstand the highest expected output voltage under both nominal and transient conditions.

The ratio of the smallest output voltage to the highest input voltage determines the smallest value of duty-cycle required from the converter. Likewise, the ratio of the highest output voltage to the lowest input voltage determines the largest value of duty-cycle required from the converter. Despite the implicit nature of the duty-cycle in the current-mode control strategy, there are secondary issues of stability requiring “slope compensation,” and minimum pulse-width control considerations, as well as other effects to be discussed.



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### 7.0 Switchmode Buck Power Converter Regulation Introduction

Practical applications typically require that we provide a controlled value for  $V_C$  despite changes in the input voltage  $V_{IN}$ . The term “line regulation” is used to describe the resulting effect of that control effort.

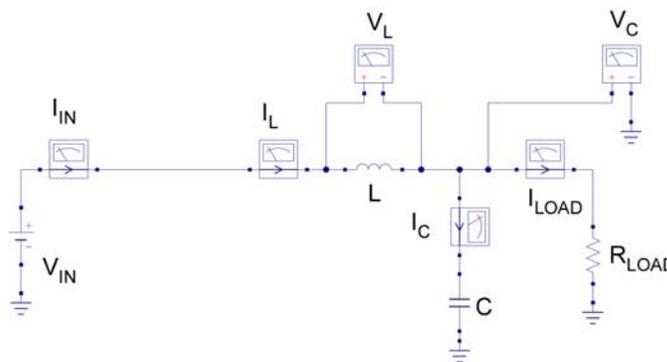
Also, practical applications require that we provide a controlled value for  $V_C$  despite changes in the load current  $I_{LOAD}$ . The term “load regulation” is used to describe the resulting effect of that control effort.

The practical applications may utilize a combination of means for controlling the duty cycle that depend both on the  $V_{IN}$  behavior, as well as the  $V_C$  behavior under changing loads. That part of the controller that utilizes the  $V_C$  behavior to control the duty cycle is called a “feedback” control mechanism. Any part of the controller that utilizes the  $V_{IN}$  behavior to control the duty cycle is called a “feedforward” control mechanism, and that mechanism is particularly difficult to explicitly implement in current-mode control, despite an inherent “feedforward” mechanism that is fundamentally part of the current-mode control approach. However, because the current-mode control uses two loops, each being first-order, an explicit feedback-only control strategy is often sufficient.

In general, feedback control requires small-signal models to determine gain and phase margins, as well as compensation required to stabilize the closed loop behavior.

### 8.0 Switchmode Buck Power Converter Regulation Model

The Buck converter model is described using two state variables: the inductor current  $I_L$  and the capacitor voltage  $V_C$ . The input voltage  $V_{IN}$  and the load resistance  $R_{LOAD}$  are retained to express the input and output dependencies for line and load regulation.



**Figure 8.0 Buck converter schematic during the  $DT$  period**



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Modeling begins with the topology defined in figure 8.0 during the *DT* interval with the input switch conducting and the diode reverse-biased, or OFF. We use Kirchoff's Voltage Law (*KVL*) around the loop including  $V_{IN}$ ,  $L$ , and  $C$ , and Kirchoff's Current Law (KCL) at the node defined by the  $V_C$  voltage, to write two defining equations:

$$V_{IN} = V_L + V_C \quad [8.0]$$

and

$$I_L = I_{LOAD} + I_C \quad [8.1]$$

Because  $V_L$ ,  $I_{LOAD}$ , and  $I_C$  are not the defined state variables, we rewrite the equations in terms of the state variables, using the Laplace "s" operator to obtain the equations:

$$V_{IN} = LsI_L + V_C \quad [8.2]$$

and

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \quad [8.3]$$

We rewrite into differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C - \frac{1}{L}V_{IN} \quad [8.4]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \quad [8.5]$$

We define a state vector composed of the two state variables:

$$X = \begin{vmatrix} I_L \\ V_C \end{vmatrix} \quad [8.6]$$

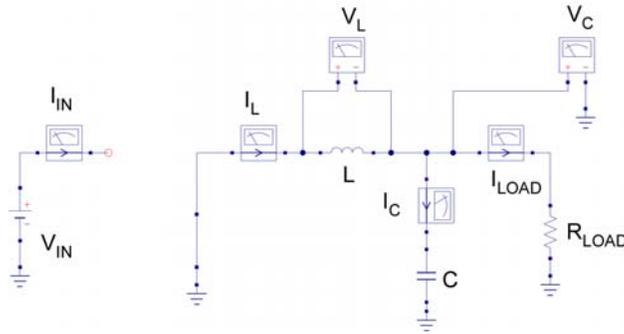
We then express the two equations in matrix form using the state vector and build the state matrix as the expression of the two simultaneous equations. It is a matrix differential equation with the derivative of the state vector  $Xs$ , expressed in terms of the state vector  $X$  itself and the  $V_{IN}$  input voltage:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN} \quad [8.7]$$



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The matrix differential equation [8.7] describes the behavior of the Buck converter during the time  $DT$  that the input supply is connected through the closed switch.



**Figure 8.1 Buck converter schematic during the  $(1-D)T$  period**

We continue modeling with the topology defined in figure 8.1, with conduction through the synchronous switch during the  $(1-D)T$  interval, again using  $KVL$  and  $KCL$  to write two modified defining equations:

$$0 = V_L + V_C \quad [8.8]$$

and

$$I_L = I_{LOAD} + I_C \quad [8.9]$$

As before, we rewrite the defining equations:

$$0 = LsI_L + V_C \quad [8.10]$$

and

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \quad [8.11]$$

We formulate into explicit differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C \quad [8.12]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \quad [8.13]$$



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Using the state vector as previously defined, we express the new matrix differential equation as follows:

$$X_S = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{bmatrix} \bullet X + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \bullet V_{IN} \quad [8.14]$$

**9.0 Switchmode Buck Power Converter State-Space Average Model**

Following the practice of state-space averaging, we sum **D** times the component matrix in equation [8.7] plus **(1-D)** times the component matrix in equation [8.14] to provide the state-space averaged equations:

$$X_S = D \begin{bmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{bmatrix} \bullet X + D \begin{bmatrix} 1/L \\ 0 \end{bmatrix} \bullet V_{IN} \\ + (1-D) \begin{bmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{bmatrix} \bullet X + (1-D) \begin{bmatrix} 0 \\ 0 \end{bmatrix} \bullet V_{IN} \quad [9.0]$$

$$X_S = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{bmatrix} \bullet X + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} \bullet DV_{IN} \quad [9.1]$$

We note that the state-space matrix term has no dependency on the duty cycle **D**, despite the alteration of the topology caused by switching. The only net effect is an explicit dependency on **D** in the source voltage alone as above in equation [9.1]:

**10.0 Switchmode Buck Power Converter Small-Signal State-Space Average Model**

We realize that the ideal component values due not change, despite the alteration of the topology and the 2x2 matrix is composed of constant values. However, the input voltage will change, the load will change, and the duty-cycle will be an implicit control variable and the state vector values will change as a consequence.

To model the small-signal behaviors, we introduce a notation that represents a DC operating point with “capital” letters, and small signal perturbations with the smaller letters for each variable and substitute in the model we developed in equation [9.1], as follows:



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$$(X + x)_s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet (X + x) + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet (D + d)(V_{IN} + v_{IN}) \quad [10.0]$$

We expand the terms, of equation [10.0], and remove any products of small terms as “second-order” and small enough to ignore, as follows:

$$X_s + x_s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet x - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X \\ + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet DV_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet dv_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} - \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet DV_{IN} \quad [10.1]$$

We can solve for the small signal state space averaged model:

$$x_s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet x + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN}d \quad [10.2]$$

The state-space averaged small-signal model is only valid for small signals. Likewise, it is only valid for small-signal perturbations that are much lower frequency than the switching frequency. Serious aliasing effects can make the model unusable for frequencies approaching a large fraction of the Nyquist frequency (half the switching frequency). However, for analysis at lower frequencies to about 10% of the switching frequency, the state-space averaged model gives good results.

**11.0 Switchmode Buck Power Converter Small-Signal Current-Mode Control**

For current programming we develop a change of control variables from the explicit duty cycle to a controlling current signal. The constraint equation is taken from the inductor current given in the first row of equation [10.2] as:

$$si_L = -1/L v_c + 1/L Dv_{IN} + 1/L V_{IN}d \quad [11.0]$$

Which we solve for d:

$$d = \frac{L}{V_{IN}} si_L + \frac{1}{V_{IN}} v_c - \frac{D}{V_{IN}} v_{IN} \quad [11.1]$$



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We substitute  $d$  back into the small-signal state space model as follows:

$$\begin{aligned} \begin{vmatrix} i_L \\ v_C \end{vmatrix} s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet \begin{vmatrix} i_L \\ v_C \end{vmatrix} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} \\ + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN} \left( \frac{L}{V_{IN}} si_L + \frac{1}{V_{IN}} v_c - \frac{D}{V_{IN}} v_{IN} \right) \end{aligned} \quad [11.2]$$

We formulate the matrix equations singly, starting with the first row:

$$si_L = -\frac{1}{L} v_c + \frac{D}{L} v_{IN} + si_L + \frac{1}{L} v_c - \frac{D}{L} v_{IN} \quad [11.3]$$

We reduce equation [11.3] to:

$$si_L = si_L \quad [11.4]$$

And from the second row, we obtain:

$$sv_C = \frac{1}{C} i_L - \frac{1}{CR_{LOAD}} v_C \quad [11.5]$$

From equation [11.5], we readily see:

$$(CR_{LOAD}s + 1)v_C = R_{LOAD}i_L \quad [11.6]$$

We obtain our final control relationship:

$$v_C = R_{LOAD} \left[ \frac{1}{CR_{LOAD}s + 1} \right] i_L \quad [11.7]$$

Armed with equation [11.7], and a means to control the inductor current  $i_L$ , we are able to control the  $v_C$  output voltage.

### 12.0 Initial Inductor Choice

We choose as a design requirement; a Buck Converter based on a nominal 10.2V to 14.7V  $V_{IN}$  range to supply 3.3V at  $V_C$  with 5 milli-Volt maximum ripple voltage. The converter must support a maximum 1 Ampere load. For contrasting illustrations, we begin with a 250 kHz switching frequency.



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We choose a peak-to-peak current ripple near 200 milli-Amperes so that we are able to discern changes in current over each portion of the cycle. The 200 milli-Ampere peak-to-peak current ripple is at least 20% of the maximum average 1 Ampere current delivered.

From the  $V_{IN}$  range and the fixed 3.3V  $V_C$  value, we can determine that the range of duty-cycle  $D$  must be 3.3/14.7 to 3.3/10.2, or 0.22 to 0.33. Knowing the range of the  $D$  duty-cycle interval, we can determine that the  $(I - D)$  interval is 0.78 to 0.67, and at 250 kHz, the times are 3.12  $\mu$ sec to 2.68  $\mu$ sec.

We use the 3.3V  $V_C$  value during the longest  $(I - D)$ , or 3.12  $\mu$ sec, interval to determine the minimum inductor value that will support that voltage with the requisite current change, as follows:

$$0.2 = \Delta I_L = \frac{V_L}{L} \Delta t = \frac{3.3}{L} 3.12 \cdot 10^{-6} \quad [12.0]$$

$$L = \frac{3.3}{0.2} \cdot 3.12 \cdot 10^{-6} = 51 \mu H \quad [12.1]$$

To further address the selection of the inductor, we must consider that the Buck converter delivers a maximum of 1A at 3.3V or 3.3Watts and should not dissipate appreciable power in the inductor, while delivering that current. The inductor must be capable of handling 1A without saturation of the inductance, as well as have a reasonably low DC resistance. The power loss in the DC resistance ( $R_L = DCR$ ) of the inductor is:

$$P = I^2 DCR \quad [12.2]$$

If we evaluate maximum loss in the inductor, that implies:

$$P_{L-Loss} = I^2 \cdot DCR \quad [12.3]$$

We find a 47  $\mu$ H Murata component (Digikey # 811-1210-2-ND) that has DC resistance of 86m $\Omega$  and will cause a 3% efficiency loss at 1 Ampere load current. Further, the 200 milli-Ampere ripple current will develop a signal of  $V_{Ripple} = I_{Ripple} \cdot R_L = 17.2$  milli-Volts for current-control feedback.

Before proceeding further, we contrast the possibility of operation at a higher switching frequency, notably at 2.5MHz rather than the 250 kHz in the prior calculations.



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The range of the  $D$  duty-cycle is unchanged, but the time intervals are shortened by a factor of 10x, so we can determine that the  $(I - D)$  interval is 0.78 to 0.67, and at 250 kHz, the times are 312 nsec to 268 nsec.

We use the 3.3V  $V_C$  value during the longest  $(I - D)$ , or 312 nsec, interval to determine the inductor value that will support that voltage with the requisite current change, as follows:

$$0.2 = \Delta I_L = \frac{V_L}{L} \Delta t = \frac{3.3}{L} 312 \cdot 10^{-9} \quad [12.4]$$

$$L = \frac{3.3}{0.1} \cdot 312 \cdot 10^{-9} = 5.1 \mu H \quad [12.5]$$

The DC resistance requirements are unchanged, and we find that we can meet the inductance with a 4.7  $\mu H$  Murata component (Digikey # 811-1251-2-ND) that has 41m $\Omega$   $\square\square$ DCR and will cause 1.4% loss at 1Ampere load current and will develop a signal of  $V_{Ripple} = I_{Ripple} * R_L = 8.2$  milli-Volts for current-control feedback.

Both inductor choices are from a Digikey on-line catalog and may be obtained from distribution. Other considerations, including price, shielding, assembly requirements, etc., can alter other component parameters, but the inductance and DCR requirements must be met by whatever selection is made.

### 13.0 The Simple Buck Converter Initial Capacitor Choice

We chose to design the example, with a 200 milli-Ampere peak-to-peak current ripple as a typical value. We determine the minimum capacitor value from the fundamental capacitor equation:

$$C = \frac{I_2 - I_1}{\Delta V_C} \Delta t \quad [13.0]$$

The 5 milli-Volt maximum ripple voltage is defined, and we have two cases for the time intervals as follows:

$$C_{250-KHz} = \frac{200 \cdot 10^{-3}}{5 \cdot 10^{-3}} \cdot 3.12 \cdot 10^{-6} = 120 \mu F \quad [13.1]$$

$$C_{2.5-MHz} = \frac{200 \cdot 10^{-3}}{5 \cdot 10^{-3}} \cdot 312 \cdot 10^{-9} = 12 \mu F \quad [13.2]$$



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We can meet the first capacitor requirements with a 6.3V 100  $\mu$ F Kemet multi-layer ceramic capacitor (Digikey # 399-5620-1-ND), or alternately at the higher frequency with a 6.3V 10  $\mu$ F Kemet multi-layer ceramic capacitor (Digikey # 399-3029-1-ND). Again, other device parameters must be considered and these selections are for illustration only.

We find that the smaller inductance and capacitance usually are less expensive and constitute one economic argument for higher frequency operation.

#### **14.0 The Buck Converter Component Choices**

We have chosen two sets of components to simultaneously meet the ripple current and output ripple voltage constraints, but at 250kHz in one case and 2.5MHz for the other. The component choices determine a second-order, LC lowpass filter, operating on the average  $DV_{IN}$  supply voltage, and the equivalent  $R_{LOAD}$  value determines the damping factor of the filter. We express the filter transfer function alone as:

$$T_{LC}(s) = \left[ \frac{1}{LCs^2 + \frac{L}{R_{LOAD}}s + 1} \right] \quad [14.0]$$

In standard form:

$$T_{LC}(s) = \frac{1}{\left( \frac{1}{\omega_0^2} s^2 + \frac{2\zeta}{\omega_0} s + 1 \right)} \quad [14.1]$$

From which we obtain:

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad [14.2]$$

$$\frac{2\zeta}{\omega_0} = \frac{L}{R_{LOAD}} = 2\zeta\sqrt{LC} \Rightarrow \zeta = \frac{1}{2R_{LOAD}} \sqrt{\frac{L}{C}} \quad [14.3]$$

From the specification to deliver 1 Ampere into the 3.3V output, we determine that:

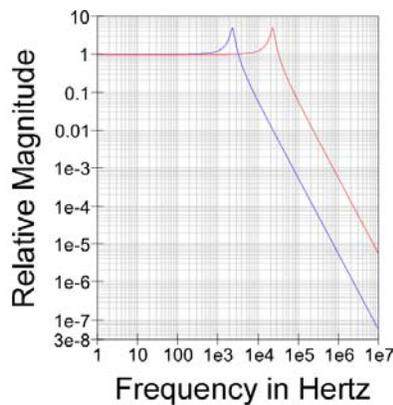
$$R_{LOAD-Min} = \frac{3.3V}{1A} = 3.3\Omega \quad [14.4]$$



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| F <sub>sw</sub> | L           | C           | $\omega_0$ | F <sub>RES</sub> | $\zeta_{Max}$ |
|-----------------|-------------|-------------|------------|------------------|---------------|
| 250 kHz         | 47 $\mu$ H  | 100 $\mu$ F | 14.6krad/s | 2.32kHz          | 0.104         |
| 2.5 MHz         | 4.7 $\mu$ H | 10 $\mu$ F  | 146 krad/s | 23.2kHz          | 0.104         |

**Table 14.0 Example LC Filter Parameters**

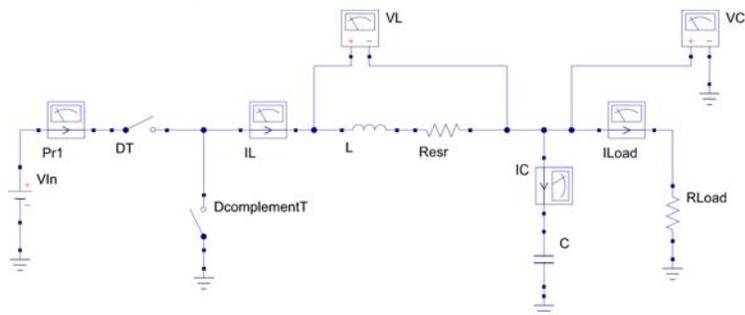


**Figure 14.0 LC Filter Magnitude Bode Plot**

We see from figure 14.0 that there is a lightly damped resonance. That resonance will present itself as an under-damped step response in the open-loop turn-on transient.

**15.0 Constructive Use of Inductor Parasitics in Current-Mode Control**

We chose inductor values, selected components from a catalog, and now discuss using the parasitic losses of the inductor as a constructive element for the signal development necessary for the current-mode control.



**Figure 15.0 Buck Converter Schematic Showing Inductor ESR**



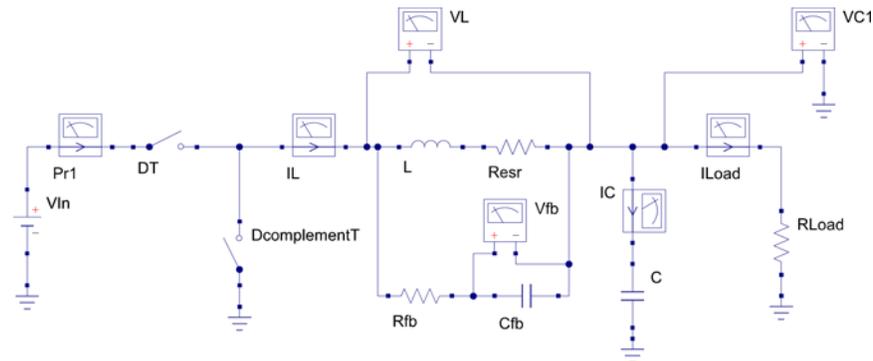
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For the series case of the inductor and its parasitic ESR resistance alone shown in figure 14.0, we write the equation for the voltage as follows:

$$V_L = (Ls + R_{esr})I_L \quad [15.0]$$

We have added the explicit component  $R_{esr}$  to the schematic in a series connection with the ideal inductor  $L$ , but the intermediate node between  $L$  and  $R_{esr}$  is not available in practice because is an integral part of the inductor itself (it is mostly the wire resistance). We could add another resistor, external to the inductor so that we can use the  $I \cdot R$  drop to indicate the inductor current. In cases requiring very precise current control, such a precision resistor makes a suitable device for obtaining the current waveform information. Instead, we discuss an alternate approach to obtaining a waveform to represent the inductor current.

To obtain the current waveform, we add two additional components, as follows:



**Figure 15.1 Buck Converter Schematic Showing Inductor ESR and  $R_{fb}$  and  $C_{fb}$**

We constrain the series impedance of the  $R_{fb}$  and  $C_{fb}$  components to be very high relative to the series impedance of the  $L$  and  $R_{esr}$  combination so that very little sensing current is drawn through the  $R_{fb}$  and  $C_{fb}$  components and solve for the  $V_{fb}$  signal as follows:

$$V_{fb} = \frac{\frac{1}{C_{fb}s}}{\frac{1}{C_{fb}s} + R_{fb}} \cdot V_L = \frac{1}{R_{fb}C_{fb}s + 1} \cdot V_L \quad [15.1]$$

We solve as follows:



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$$V_{fb} = \frac{1}{R_{fb} C_{fb} s + 1} \bullet (Ls + R_{esr}) I_L \quad [15.2]$$

$$V_{fb} = \frac{\frac{L}{R_{esr}} s + 1}{R_{fb} C_{fb} s + 1} \bullet R_{esr} I_L \quad [15.3]$$

If we carefully “tune” the  $R_{fb}$  and  $C_{fb}$  product to nearly equal the  $L$  to  $R_{esr}$  ratio, a pole-zero cancellation occurs and

$$V_{fb} = \frac{\frac{L}{R_{esr}} s + 1}{R_{fb} C_{fb} s + 1} \bullet R_{esr} I_L \cong R_{esr} I_L \quad [15.4]$$

In practice, the cancellation is sufficient for current-mode control. The implementation requires a high-speed differential amplifier to develop the  $V_{fb}$  signal but the requirements are reasonable for most implementations. As an alternate sensing approach, a small explicit resistor could always be added in series with the inductor.

We evaluate the  $R_{fb}$  and  $C_{fb}$  components associated with the inductor selection in the following discussion. The 47  $\mu\text{H}$  Murata component (Digikey # 811-1210-1-ND) that has DC resistance of 86m $\Omega$  evaluates to the  $L$  to  $R_{esr}$  ratio time constant:

$$\frac{L}{R_{esr}} = \frac{47 \bullet 10^{-6}}{86 \bullet 10^{-3}} = 546 \bullet 10^{-6} \quad [15.5]$$

To meet this equivalent  $R_{fb}$  and  $C_{fb}$  component time constant, while choosing the value of  $R_{fb} = 100 \text{ k}\Omega$ , we have:

$$\frac{L}{R_{esr}} = 546 \bullet 10^{-6} = 100 \bullet 10^{-3} C_{fb} \quad [15.6]$$

$$C_{fb} = \frac{546 \bullet 10^{-6}}{100 \bullet 10^3} = 5.460 \bullet 10^{-9} = 5460 \text{ pF} \quad [15.7]$$

The 4.7  $\mu\text{H}$  Murata component (Digikey # 811-1251-2-ND) that has DC resistance of 41m $\Omega$  evaluates to the  $L$  to  $R_{esr}$  ratio time constant:



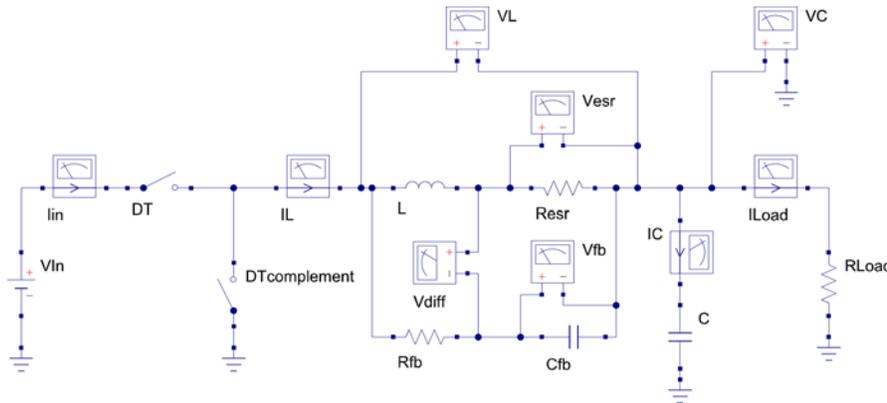
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$$\frac{L}{R_{esr}} = \frac{4.7 \cdot 10^{-6}}{41 \cdot 10^{-3}} = 115 \cdot 10^{-6} \quad [15.8]$$

To meet this equivalent  $R_{fb}$  and  $C_{fb}$  component time constant, while choosing the value of  $R_{fb} = 100 \text{ k}\Omega$ , we have:

$$\frac{L}{R_{esr}} = 115 \cdot 10^{-6} = 100 \cdot 10^{-3} C_{fb} \quad [15.9]$$

$$C_{fb} = \frac{115 \cdot 10^{-6}}{100 \cdot 10^3} = 1.15 \cdot 10^{-9} = 1150 \text{ pF} \quad [15.10]$$



**Figure 15.2 Buck Converter Schematic Showing Inductor  $V_{esr}$ ,  $V_{fb}$  and  $V_{diff}$**

We illustrate with an open-loop Buck converter simulation with  $V_{IN} = 12\text{V}$ , and a fixed duty cycle  $D = 3.3/12 = 0.275$  to obtain a 3.3V output at  $V_C$ . The value of  $R_{Load}$  is a fixed  $3.3 \Omega$  resistor and the resulting load current is  $3.3\text{V}/3.3 \Omega = 1$  Ampere.

The  $V_{IN} = 12\text{V}$  appears as a step excitation to the LC filters (previously illustrated in the frequency domain in figure 14.0), and results in similar transient responses with the same damping factor but a 10x difference in time scale due to the different resonant frequency of each implementation. Adjacent illustrations place the network with LC components for 250 kHz switching on the left, and LC components for 2.5 MHz switching on the right. The transient response for 2.5 MHz switching settles ten times faster ( $< 1$  milli-second) than the 250 kHz switching response, although both settle at 3.3V ultimately. In figure 15.3 below, the open-loop transient response effect on the  $V_C$  output voltage is clear.



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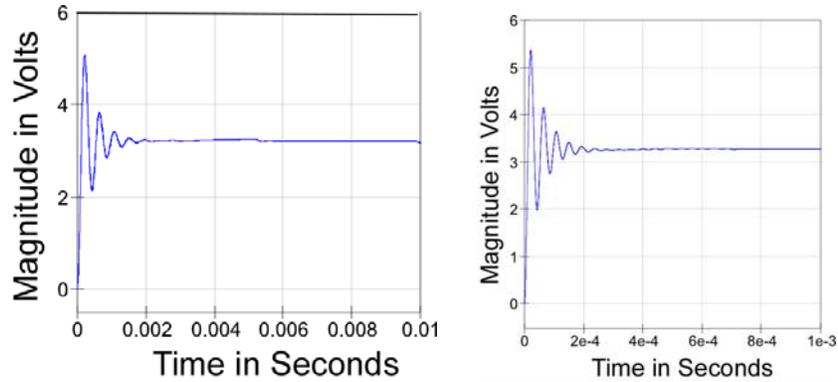


Figure 15.3 Buck Converter Open-Loop  $V_C$  Output Voltage Transient

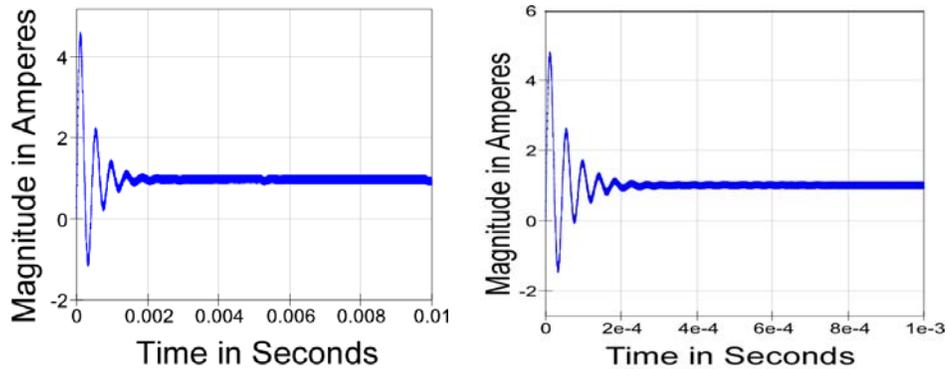


Figure 15.4 Buck Converter  $I_L$  Inductor Current Transients

Above, in figure 15.4, the open-loop transient responses of the  $I_L$  inductor current is similar in shape to the  $V_C$  output voltage transient but includes the ripple current superimposed on the average current.

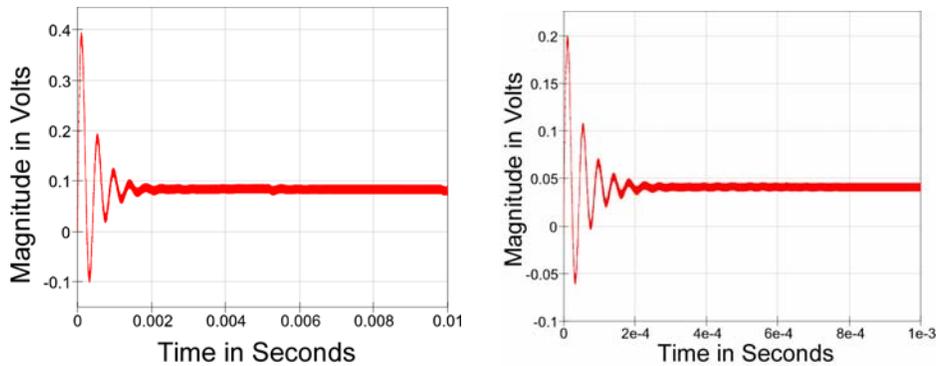


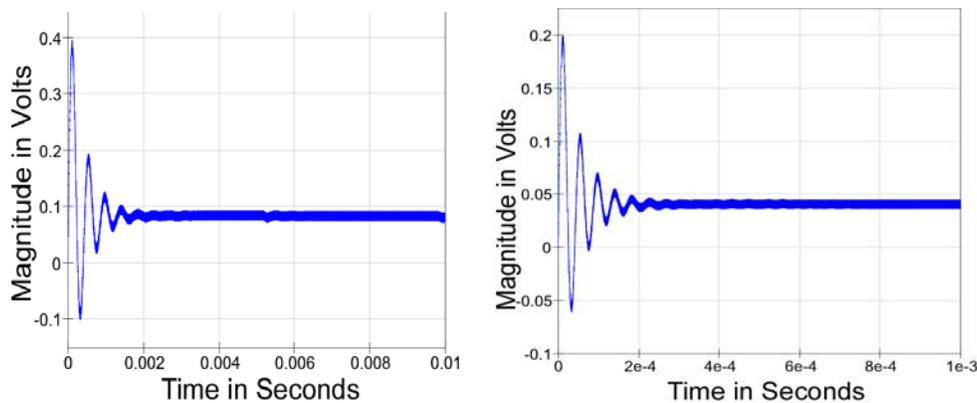
Figure 15.5 Buck Converter Inductor  $V_{esr}$  Voltage Drops



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We placed an explicit  $R_{esr}$  resistor in the simulation schematic of figure 15.2 to produce the simulated  $V_{esr}$  voltage drop. Above, in figure 15.5, the  $I_L$  inductor current causes the  $V_{esr}$  voltage drop with a scale factor of  $R_{esr}$  Volts per Ampere of  $I_L$  inductor current. The 47  $\mu\text{H}$  Murata component (Digikey # 811-1210-1-ND) with DC resistance of 86m $\Omega$  switching at 250 kHz produces 86 milli-Volts per Ampere of  $I_L$  inductor current in the illustration to the left. The 4.7  $\mu\text{H}$  Murata component (Digikey # 811-1251-2-ND) with DC resistance of 41m $\Omega$  and 2.5 MHz switching produces 41 milli-Volts per Ampere of  $I_L$  inductor current in the illustration to the right. The waveforms in figure 15.5 are available in the simulation but cannot be obtained from direct measurements.

We also placed an explicit  $R_{fb}$  resistor and  $C_{fb}$  capacitor in the simulation schematic shown in figure 15.2 to allow development of the simulated  $V_{fb}$  voltage drop that is shown in figure 15.6 below. The waveforms in figure 15.6 are available in the simulation but can also be obtained from direct component measurements. For 250 kHz switching, the 100k $\Omega$   $R_{fb}$  resistor with 5460 pF  $C_{fb}$  capacitor produces a  $V_{fb}$  of 86 milli-Volts per Ampere of  $I_L$  inductor current in the illustration to the left. For 2.5 MHz switching, the 100k $\Omega$   $R_{fb}$  resistor with 1150 pF  $C_{fb}$  capacitor produces a  $V_{fb}$  of 41 milli-Volts per Ampere of  $I_L$  inductor current in the illustration to the right.

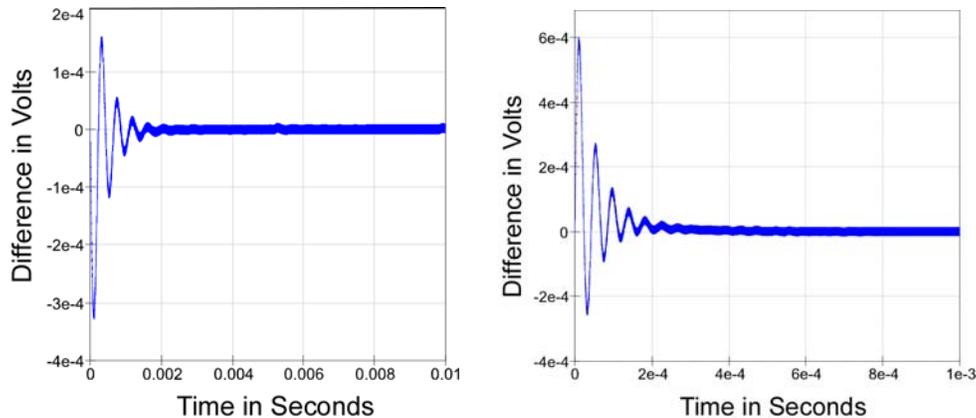


**Figure 15.6 Buck Converter Inductor RC Sense Network Voltage Drops**

We have claimed that the equation 15.4 above directs us to the explicit  $R_{fb}$  resistor and  $C_{fb}$  capacitor values that will tune the  $V_{fb}$  signal response to be identical to the unavailable  $V_{esr}$  voltage drop. To validate the claim, we have simulated the signal  $V_{diff}$  from figure 15.2, and illustrated in figure 15.7 below for both switching frequencies and  $R_{fb}$  resistor and  $C_{fb}$  capacitor sets.



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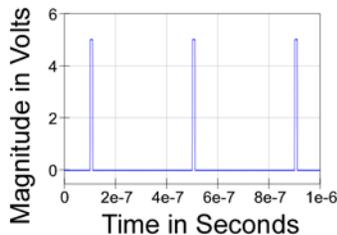


**Figure 15.7 Buck Converter  $V_{diff} = V_{esr} - V_{fb}$  Simulation Differences**

Results shown in figure 15.7 indicate that the  $V_{fb}$  signal can be employed to represent the unavailable equivalent  $V_{esr}$  signal with less than 1% error. Direct DC measurement of the  $R_{esr}$  inductor resistance and selection of the  $R_{fb}$  resistor and  $C_{fb}$  capacitor components may be required to obtain such accuracy, but there is nothing preventing the employment of the signal strategy in theory. Accuracy of 10% or even worse may be acceptable for many applications.

### 16.0 Constant Frequency Timing in Current-Mode Control

We provide a constant-frequency pulse-oscillator timing reference as shown in figure 16.0 from which we develop our controller timing. From here onward, we use only the 2.5 MHz switching example to avoid confusion in the sections that follow, but the principles are the same for any frequency chosen.



**Figure 16.0 2.5MHz Pulse Oscillator Timing Reference (400 nanosecond  $T_S$ )**

From the pulse oscillator, shown with a 5Volt logic-level and a 10 nano-second logic high period, we derive two delayed versions shown in figure 16.1, one designated with a short delay, and the second with a longer delay relative to the pulse oscillator reference waveform itself.



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**Figure 16.1 The 2.5MHz Pulse Oscillator with Two Delayed Replicas**

The two delayed versions shown in figure 16.1, one designated with a short delay, and the second with a longer delay relative to the pulse oscillator reference waveform improve timing accuracy for control purposes. We have shown the short delay of the first replica with a 20 nano-second delay from the pulse oscillator waveform, and the long delay of the second replica with a 40 nano-second delay from the pulse oscillator waveform. Implementations that control timing of these delays is possible with less than 10% uncertainty of each delay.

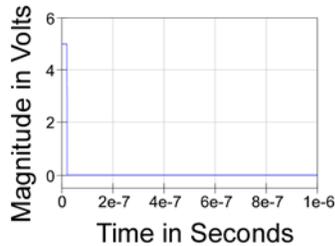
The implementation may produce the pulse designated as the longer delay relative to the pulse oscillator by applying a delay to the pulse designated as the shorter delay to ensure the strict sequence of pulses. We will define the delay between the pulse oscillator and the pulse designated as the shorter delay as  $T_{off}$  for reasons that will become apparent. Further, we define the delay between pulse designated as the shorter delay and the pulse designated as the longer delay as  $T_{on-Min}$  for reasons that will also become apparent.

We employ a Flip/Flop as a Pulse-Width Modulator (PWM). We initiate all PWM periods with the “short” delay waveform relative to the pulse oscillator waveform. In each PWM period the initiation by the “short” delay waveform is called  $T_{Start}$ . The period of the PWM is controlled so that it terminates on one of three events, the waveform designated as the “long” delay waveform, the next pulse oscillator pulse that occurs, or a pulse that occurs between the two.

To initialize the PWM Flip/Flop, we employ a reset pulse shown in figure 16.2 that is derived from start-up logic designating that a logic high means the implementation is not ready and conversely the logic low enables the PWM Flip/Flop.

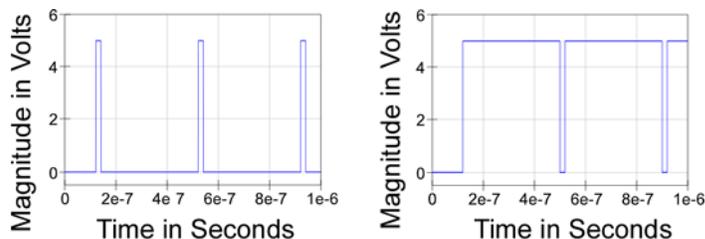


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**Figure 16.2 The Supervisory “Reset” Signal to Permit Timing to Commence**

The PWM Flip/Flop is initialized with its output in the logic low by the supervisory signal, as shown in figure 16.3, and limited between the shortest and longest pulses displayed in figure 16.3 below.



**Figure 16.3 The PWM Shortest and Longest Pulses Supported at Constant  $T_S$**

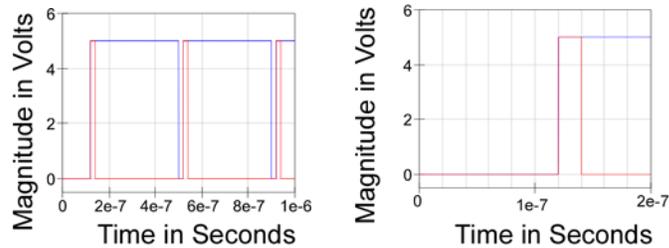
The PWM Flip/Flop is initialized with its output in the logic low by the supervisory signal, as shown in figure 16.3, and limited between a shortest and longest pulse. Each PWM period begins at the  $T_{Start}$  instant, corresponding to the pulse with the “short” delay of the pulse oscillator.

The shortest PWM pulse occurs between that  $T_{Start}$  instant and the next following “long” delay pulse. We have already defined the delay between pulse designated as the shorter delay and the pulse designated as the longer delay as  $T_{on-Min}$  for reasons that now become apparent.

The longest PWM pulse occurs between the  $T_{Start}$  instant and the next following pulse oscillator pulse. We have already defined the delay between pulse oscillator and the next  $T_{Start}$  instant as  $T_{off-Min}$  for reasons that now become apparent because the PWM has a logic low signal in that interval.



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**Figure 16.3 The PWM Shortest and Longest Pulses Superimposed at Constant  $T_S$**

The shortest and longest PWM pulses are not available simultaneously, but are shown above in figure 16.3 to illustrate that PWM pulses are all initiated at the  $T_{Start}$  instant and defined between limits imposed by the  $T_{on-Min}$  and  $T_{off-Min}$  time intervals. The 20 nano-second delays employed are reasonable, but can be changed to suit the circumstances.

We can translate the  $T_{on-Min}$  and  $T_{off-Min}$  time intervals into equivalent limits on the PWM duty cycle  $D$ , as follows:

$$D_{Min} = \frac{T_{on-Min}}{T_S} \quad [17.0]$$

$$D_{Max} = \frac{T_S - T_{off-Min}}{T_S} \quad [17.1]$$

The implementation of the delays associated with the  $T_{on-Min}$  and  $T_{off-Min}$  time intervals ensures that precision is easily attained.

In other implementations, the  $T_{on-Min}$  and  $T_{off-Min}$  time intervals may be permitted to include zero delay. Under conditions of  $T_{on-Min}$  (or  $T_{off-Min}$ ) = 0, the duty cycle is allowed to include 0% (or 100%) and the result is called “pulse-skipping.” The pulse-skipping can increase efficiency under light loads, but the benefits of constant frequency are lost and Electromagnetic Interference (EMI) can easily result with pulsing modulated by the load conditions.

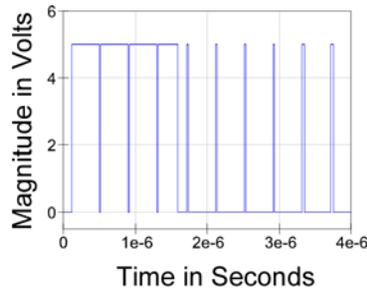
### 18.0 Current Limit Control

Using the  $V_{fb}$  signal developed from the  $R_{fb}$  resistor and  $C_{fb}$  capacitor, and characterized by the 41 milli-Volts per Ampere of  $I_L$  inductor current for the 2.5 MHz switching example, we include a simple comparator with a DC threshold for a current limit. For example, a 41 milli-Volt threshold could be used to indicate that the inductor current exceeds 1 Ampere. Similarly, an 82 milli-Volt threshold could be used to indicate that the inductor current exceeds 2 Amperes. We choose to implement 1.5 Ampere current



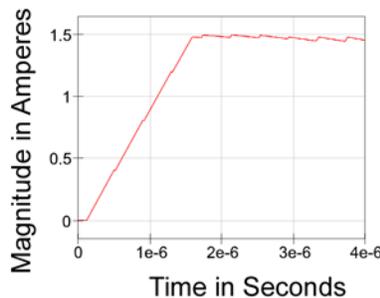
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limiting for service with the 1.0 Ampere output nominal maximum to support ripple excursions above the average current level.



**Figure 18.0 The PWM Various Pulses During Current Limit Control**

In figure 18.0 above, we utilize the PWM signal to control switching for the open-loop Buck converter. The first few cycles increase current flow in the inductor as shown in figure 18.1 below, until the 1.5 Ampere current limit is encountered.

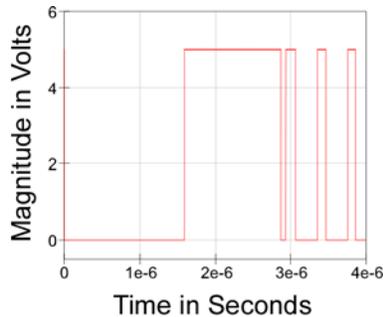


**Figure 18.1 The Buck Converter Inductor Current During Current Limit Control**

The inductor current increases whenever the PWM signal is logic high, and decreases whenever it is logic low, according to the normal operation of the Buck converter, consequently, the current limit is crossed while the PWM signal is logic high. We see the asynchronous nature of the current limit comparator switching below in figure 18.2, both for the initial period and several events thereafter.

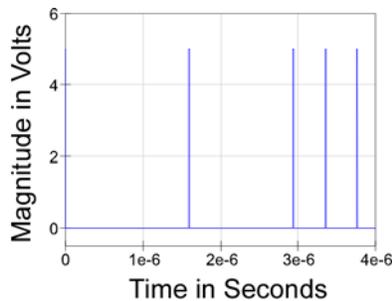


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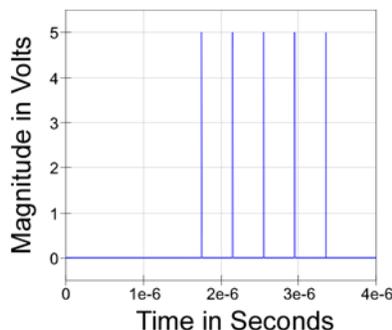
**Figure 18.2 The Current Limit Comparator Asynchronous Switching**

Because the current limit comparator switches asynchronously, we develop a pulse from the rising edge of the comparator signal as shown in figure 18.3 below, and use it to terminate any PWM period during which the edge occurs.



**Figure 18.3 The Current Limit Comparator Asynchronous Rising Edge Pulses**

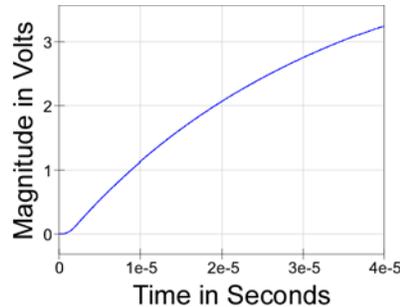
We see in figures 18.1 and 18.2 that an extended period of several cycles occurs with the current somewhat higher than the limit and the comparator continues to indicate an over-current condition. We use the logic high developed by the comparator to initiate PWM switching with a period of  $T_{on-Min}$  during each cycle as shown in figure 18.4 below.



**Figure 18.4 Switching with  $T_{on-Min}$  During Over-Limit Periods**



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**Figure 18.5  $V_C$  Output Voltage During the Current-Limit Control**

In figure 18.5, we see that the output voltage is uncontrolled and ultimately approaches the asymptotic level of  $I_{Limit} * R_{Load} = 4.95$  Volts, far above the target of 3.3 Volts specified. It is clear, however, that we can establish another current limit below the maximum current limit shown above and manipulate its value under feedback control to establish voltage regulation. We will leave the current limit behavior above for those instances when a short-circuit, or other fault condition is encountered.

### 19.0 Pulse-by-Pulse Current Control

We return to the small-signal relationship of equation [11.7], and repeated here for convenience as:

$$v_C = R_{LOAD} \left[ \frac{1}{CR_{LOAD}s + 1} \right] i_L \quad [11.7]$$

It is clear that our strategy of controlling the inductor current allows control of the output voltage, both as the large-signal  $V_C$ , and the small-signal perturbations  $v_C$  around the desired operating point.

Referring to the  $V_{fb}$  signal developed from the  $R_{fb}$  resistor and  $C_{fb}$  capacitor, and characterized by the 41 milli-Volts per Ampere of  $I_L$  inductor current for the 2.5 MHz switching example, we can induce that the same voltage value must be applied at the comparator input to obtain that peak current. We recognize that the peak current differs from the average current, but the peak current is equal to the average plus half the peak-to-peak ripple current. We have shown that the ripple current is a function of the duty-cycle but not the average current, so we treat the half-ripple as an offset and retain the 41 milli-Volts per Ampere of  $I_L$  inductor current as an incremental relationship for programming the current-control.

We find that the programming relationship is better expressed as the ratio:

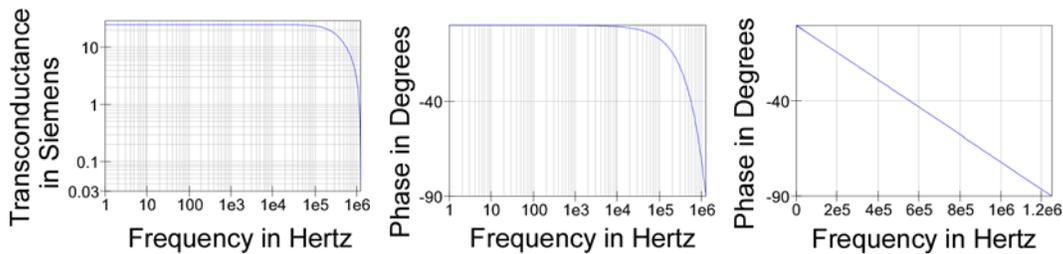


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$$\Delta I_L = G_{PWM} \cdot \Delta V_{Control} \quad [19.0]$$

$$G_{PWM} = \frac{\Delta I_L}{\Delta V_{Control}} = \frac{1 \text{Ampere}}{0.041 \text{Volts}} = 24.4 \text{Siemens} \quad [19.1]$$

The 24.4 Siemens equivalent transconductance is obtained by making incremental voltage-level changes at the input to the comparator. Because that voltage is translated by a discrete-time sampling of currents, it is not frequency independent, but rather follows the characteristics of a Zero-Order Hold (ZOH) with the 2.5 MHz sampling rate.



**Figure 19.0 Current Control Transconductance Bode Plots**

Sampling using the inherent Zero-Order Hold (ZOH) caused by the PWM 2.5 MHz switching rate results in the deep notch in the transconductance at the 1.25MHz Nyquist rate. The ZOH also introduces the delay that results in the constant phase slope shown on the far right. Plotted on the same logarithmic frequency scale as the magnitude, the phase shift is most significant in the last decade before the Nyquist frequency. The ZOH phase shift, along with its magnitude effects, alters the open-loop feedback transfer function and must be considered in faster, wide-bandwidth control loops. The ZOH effects prevent feedback control at higher frequencies than or approaching the Nyquist rate.

We return to equation [11.7], and include the effects of the ZOH as follows:

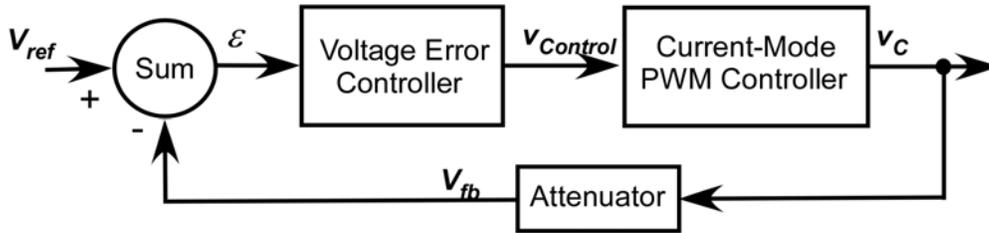
$$v_C = R_{LOAD} \left[ \frac{1}{CR_{LOAD}s + 1} \right] i_L = R_{LOAD} \left[ \frac{1}{CR_{LOAD}s + 1} \right] G_{PWM} T_{ZOH} v_{Control} \quad [19.2]$$

$$\frac{v_C}{v_{Control}} = R_{LOAD} \left[ \frac{1}{CR_{LOAD}s + 1} \right] G_{PWM} T_{ZOH} = T_{Current-Control} (s) \quad [19.3]$$



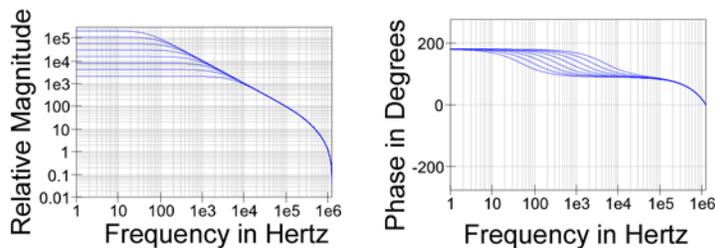
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The transfer function from the control voltage to the output capacitor voltage is designated as  $T_{Current-Control}(s)$ , and is shown as the “inner-loop” as the “Current-Mode PWM Controller” in figure 19.1 below:



**Figure 19.1 Current Control Inner/Outer Loop Feedback Structure**

The transfer function designated as  $T_{Current-Control}(s)$  is frequency dependent both from the action of the ZOH, the DC gain shift from the  $G_{PWM}R_{Load}$  product, and the  $CR_{Load}$  output pole. Because the effects of the DC gain shift from the  $R_{Load}$  dependency, and the  $R_{Load}$  output pole dependency alter the bandwidth in opposite directions, the Gain-Bandwidth product (GBW) remains constant as shown in figure 19.2 below. The single pole phase shift, however, is a different matter and must be considered in the voltage feedback control employed.



**Figure 19.2 Current Control Inner Loop Bode Plots**

In figure 19.2, the value of  $R_{Load}$  is swept between  $330\ \Omega$  and  $3.3\ \Omega$ , corresponding to a variation in load current over 1:100 range from 10 milli-Amperes to the full 1 Ampere required. The attenuator shown in figure 19.1 is connected directly to the  $V_C$  output and may be configured a  $330\ \Omega$  resistive divider ensuring a minimum load is always present.

To complete the open-loop around an “outer” voltage feedback portion, we add the attenuator and the voltage-error controller. The “Voltage Error Controller” component consists of an integrator and a single pole-zero (PZ) network with the transfer function described in equation [19.4} below:

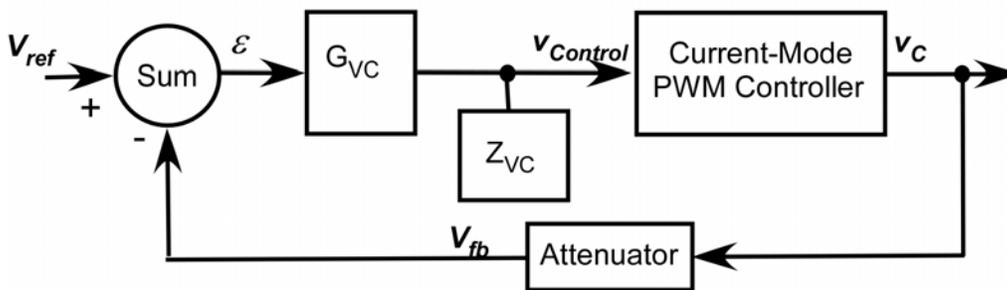


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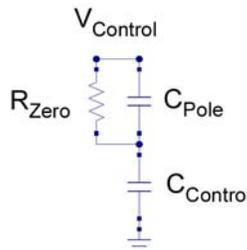
$$\frac{v_{Control}}{\varepsilon} = \frac{G_{VC}}{C_{Control}s} \left[ \frac{\tau_{Zero}s + 1}{\tau_{Pole}s + 1} \right] = G_{VC} \cdot \frac{1}{C_{Control}s} \left[ \frac{R_{Zero} C_{Zero}s + 1}{R_{Zero} C_{Pole}s + 1} \right] = G_{VC} \cdot Z_{VC} \quad [19.4]$$

The particular form of equation [19.4] supports an implementation consisting of a transconductance with value  $G_{VC}$ , followed by a passive network  $Z_{VC}$  at the  $V_{Control}$  node.

That form of implementation supports the use of a single design that can be “tuned” connecting passive components at a single node as follows:



**Figure 19.3 Current Control Inner/Outer Loop Feedback with  $G_{VC} \cdot Z_{VC}$  Structure**



**Figure 19.4  $Z_{VC}$  Structure Schematic**

$$Z_{VC} = \frac{1}{C_{Control}s} \left[ \frac{R_{Zero} (C_{Control} + C_{Pole})s + 1}{R_{Zero} C_{Pole}s + 1} \right] \quad [19.5]$$

For the values of  $C_{Control} = 0.1\mu\text{F}$ ,  $C_{Pole} = 300\text{ pF}$ , and  $R_{Zero} = 1000\ \Omega$ , we have a  $\tau_{Zero}$  associated with 1.6 kHz, and a  $\tau_{Pole}$  associated with 530 kHz. The associated  $G_{VC}$  value is  $6.3 \cdot 10^{-3}$  Siemens, which makes the  $G_{VC}/C_{Control}$  integrator pole = 10 kHz and as is shown in the Bode plots of figure 19.5 as follows:



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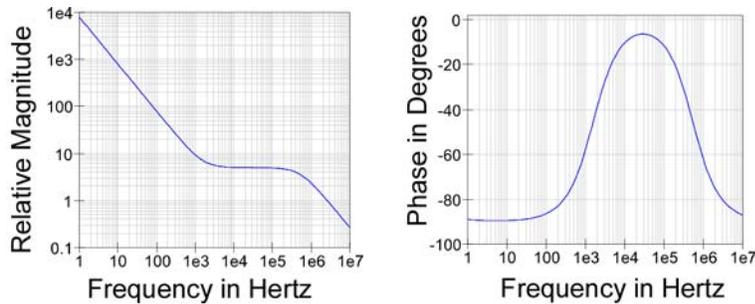


Figure 19.5  $G_{VC} * Z_{VC}$  Structure Bode Plots

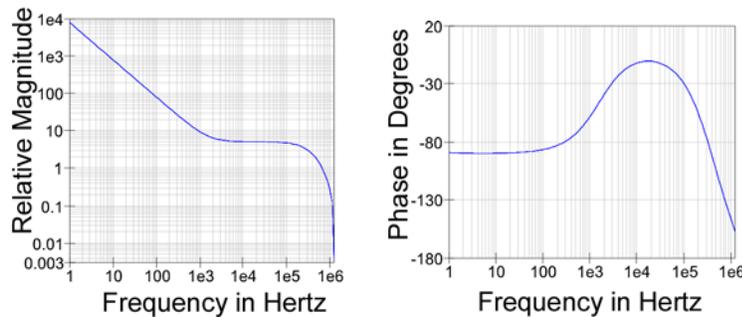


Figure 19.5  $G_{VC} * Z_{VC}$  Structure Bode Plots with ZOH Magnitude and Phase included

Combining the  $G_{VC} * Z_{VC}$  Bode Plot behavior with the Current Control Inner Loop Bode Plot behaviors, we obtain most of the open-loop behavior Bode Plots as follows:

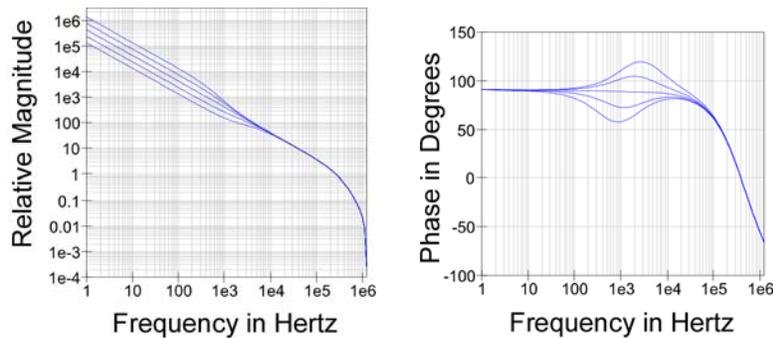


Figure 19.6 Current Combined Inner/Outer Open-Loop Bode Plots

The particular choice of component values at the  $V_{Control}$  node, with the  $G_{VC}$  choice, produces a unity-gain frequency of greater than 200 kHz with a phase margin approximately  $50^\circ$  at that frequency. If we combine a DC gain in the differential error

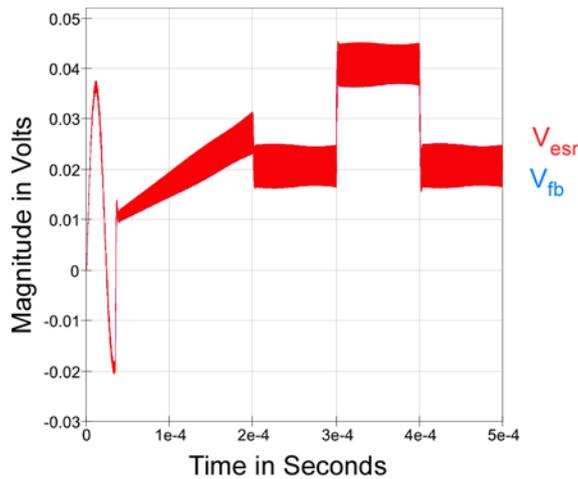


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amplifier/Sum function that is equal to the attenuator loss, there will be no effect on the stability and the loop can be closed.

### 20.0 Closed Loop Current Control

We close the loop shown in figure 19.3 and provide two “soft-start” signals to the PWM comparator, one to initiate a ramp of the ILIM current limit so that the maximum current limit begins at zero and reaches a maximum of 2Amperes at 10  $\mu$ sec, and a second ramp of the  $V_{ref}$  signal that begins at zero and reaches the regulation  $V_C$  target of 3.3 Volts at 200  $\mu$ sec. The “soft-start” implementation supports a controlled level of current demanded from the  $V_{IN}$  supply that is less than the ILIM maximum current limit. The simulation is run with two independent comparators so that the ILIM control can be contrasted with the PWM current control in the following discussion. The functions can be merged so that a single comparator can be employed, but that makes comparing the limiting actions more difficult.

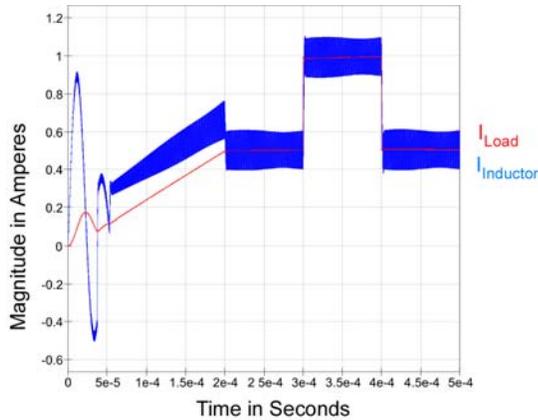


**Figure 20.0 Buck Converter  $V_{esr}$  and  $V_{fb}$  Simulation Signals**

In figure 20.0, we superimpose the  $V_{fb}$  signal developed from the  $R_{fb}$  resistor and  $C_{fb}$  capacitor, and characterized by the 41 milli-Volts per Ampere of  $I_L$  inductor current for the 2.5 MHz switching example with the simulated  $I_L * R_{esr}$  product designated as the  $V_{esr}$  signal. As before, they are indistinguishable, and the  $V_{fb}$  signal is employed for both ILIM and PWM control.

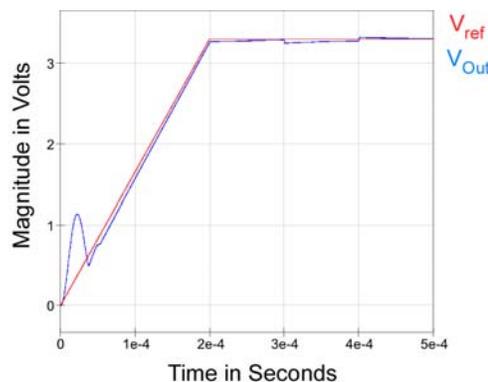


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**Figure 20.1 Buck Converter Inductor and Load Current Signals**

In figure 20.1, we show the  $I_L$  inductor current-controlled waveform with the  $V_{Load}$  signal during the “soft-start” charging interval, as well as during the constant  $V_{Out}$  interval including the load step sub-interval.. Below, in figure 20.2, we show the resulting  $V_C$  output voltage waveform, as well as the  $V_{ref}$  control target waveform. We have been careful to “tune” the “soft-start” ramp rates for the current target and the voltage target to obtain an effect near the result of a single-comparator design yet retaining the separation of the ILIM and voltage control PWM functions. Below, in figure 20.2, the reference  $V_{ref}$  control target and  $V_C$  output voltage slopes nearly match for the first 200  $\mu$ second interval. The combined sum of the current delivered to the load as shown in figure 20.1 and the current absorbed charging the 10 $\mu$ F output capacitor is equal to the inductor current during the “soft-start” ramp.

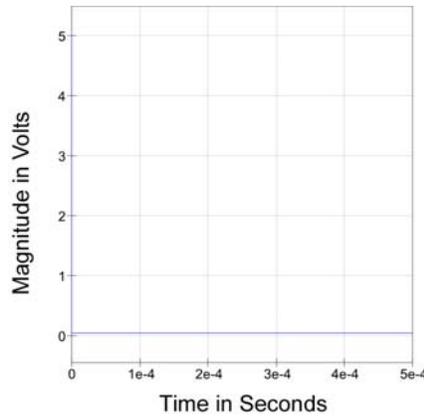


**Figure 20.2 Buck Converter Controlled  $V_{ref}$  Target and  $V_{Out}$  Signals**



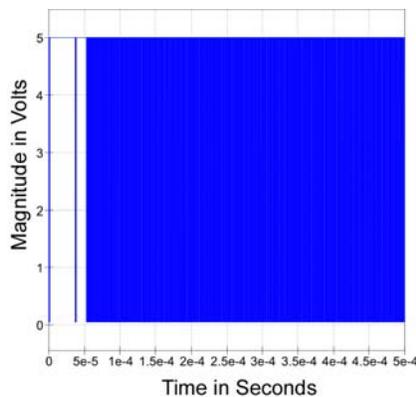
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We have retained the ILIM comparator as discussed in section 18.0 above and added an independent PWM current comparator controlled by the voltage error signal as discussed in section 19.0 above, we have signals that indicate when the ILIM level is controlling, and a distinct signal indicating when the voltage error is controlling, as shown in figures 20.3 and 20.4 below.



**Figure 20.3 Buck Converter ILIM PWM Current Control Signals**

In figure 20.3, we show the ILIM comparator signals indicate that the current never reached the programmed ILIM limit. The presence of pulses could be expected if the output were subjected to an overload condition.



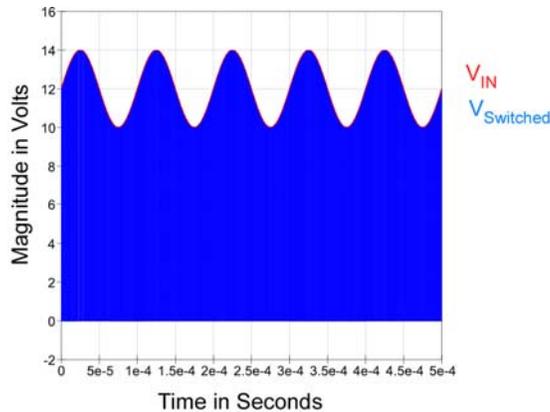
**Figure 20.4 Buck Converter Voltage Error PWM Current-Control Signals**

During the “soft-start” ramp, and after the output  $V_C$  voltage exceeds the  $V_{ref}$  target, the control is entirely determined by the voltage error comparator shown in figure 20.4 above.

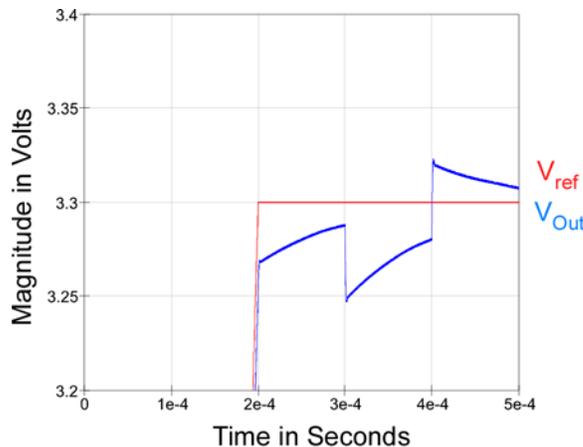


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For the entire control interval using current-mode control, we have included a 4 Volt peak-to-peak 10KHz sinusoidal variation of the  $V_{IN}$  supply voltage as shown below in figure 20.5 to demonstrate the reasonably good line regulation of the current-mode control approach.



**Figure 20.5 Buck Converter  $V_{IN}$  Supply and Switched PWM Signals**



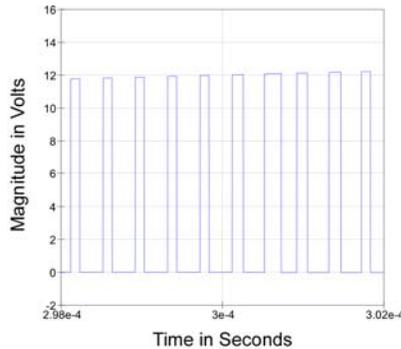
**Figure 20.6 Buck Converter Controlled  $V_{ref}$  Target and  $V_{Out}$  Signal Details**

In figure 20.6, we see no noticeable effect of the supply variation, but we do notice a step change in the regulated voltage in response to the  $R_{Load}$  current step from 0.5 Ampere to 1.0 Ampere at the 300  $\mu$ second mark, and again at the return to 0.5 Ampere at the 400  $\mu$ second mark. Despite the voltage response to the load variation, there is very little change in the requisite PWM duty cycle at the transitions as shown in figures 20.7 and 20.8 below, but a subtle variation in the peak-to-peak Ripple currents can be detected at

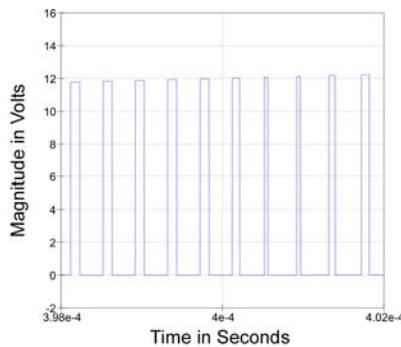


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the sinusoidal rate with a careful inspection of the  $I_L$  inductor current in figure 20.1 above.



**Figure 20.7 Buck Converter PWM duty-cycle variation with  $I_{Load}$  Increased**



**Figure 20.8 Buck Converter PWM duty-cycle variation with  $I_{Load}$  Decreased**

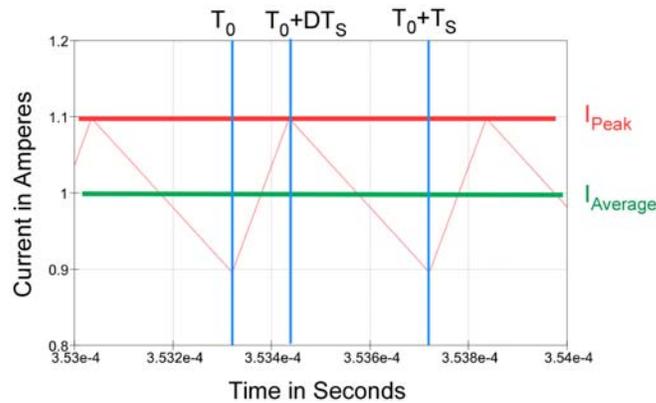
### **21.0 Slope Compensation**

Current-mode control introduces instability issues if the application requires a duty-cycle greater than 50% at the nominal operating point. We have developed the example with a duty-cycle less than 50% at the nominal operating point and avoided the issue. In this section we show how the issue arises and one method of “Slope Compensation” for decreasing the instability, including an optimal solution that provides fast correction for small signal errors.

In figure 21.0 below, we show a detail of the inductor current with a 1 Ampere average current delivered and the implied equivalent  $I_{Peak}$  comparator level that controls the switching cycle.

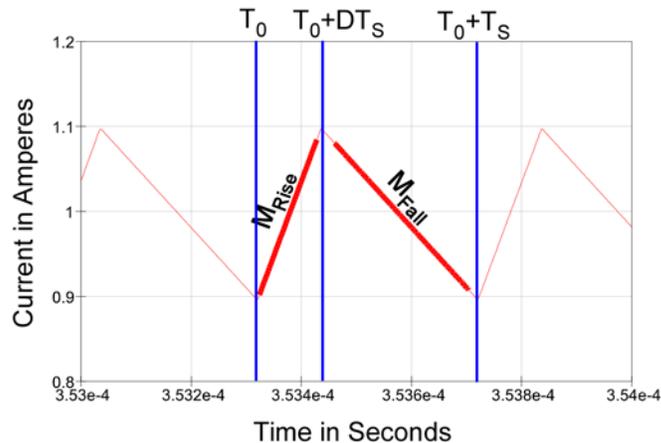


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**Figure 21.0 Peak Current Switching in Current-Mode Control**

PWM switching is initiated by the pulse oscillator at the event marked as  $T_0$ , and every subsequent event with a  $T_S$  switching period. The PWM interval between  $T_0$  and  $T_0 + DT_S$  corresponds to the  $I_L$  inductor current rising. The crossing of the  $I_L$  inductor current through the implied equivalent  $I_{Peak}$  comparator level is the signal for switching the PWM to the remainder of the cycle indicated by the  $I_L$  inductor current falling until the next cycle initiated by the pulse oscillator at the next  $T_0 + T_S$  event. The sequence of PWM events initiated by the pulse oscillator and terminated by the comparator is repeated. The implied equivalent  $I_{Peak}$  comparator level controls the cycle-by-cycle current level.



**Figure 21.1 Current-Mode Control Waveform Slopes**

We designate the slope of the  $I_L$  inductor rising current during the  $T_0$  to  $T_0 + DT_S$  interval as  $M_{Rise}$ , and the slope of the  $I_L$  inductor falling current during the  $T_0 + DT_S$  to  $T_0 + T_S$  interval as  $M_{Fall}$ , with the associated evaluations as follows:



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$$M_{Rise} = \frac{V_{IN} - V_C}{L} \quad [21.0]$$

$$M_{Fall} = \frac{-V_C}{L} \quad [21.1]$$

Because the Buck converter voltages determine the slopes, both nominal and small-signal incremental changes can be expected during each interval.

$$M_{Rise} + m_{Rise} = \frac{V_{IN} + v_{IN} - V_C - v_C}{L} \quad [21.3]$$

$$M_{Fall} + m_{Fall} = \frac{-V_C - v_C}{L} \quad [21.4]$$

We find the small-signal incremental changes as follows:

$$(M_{Rise} + m_{Rise}) - M_{Rise} = m_{Rise} = \left( \frac{V_{IN} + v_{IN} - V_C - v_C}{L} \right) - \frac{V_{IN} - V_C}{L} = \frac{v_{IN} - v_C}{L} \quad [21.5]$$

$$(M_{Fall} + m_{Fall}) - M_{Fall} = m_{Fall} = \frac{-V_C - v_C}{L} - \frac{-V_C}{L} = \frac{-v_C}{L} \quad [21.6]$$

In equation [21.5] we find that the slope depends on the  $V_{IN}$  variations, both in large and small-signal dependencies. We have no control over the  $V_{IN}$  variations and treat the signals as exogenous and show the system response to those signals. Because the  $V_C$  output voltage is internally controlled by the feedback, we ignore the effects of that variation.

We show the remaining small-signal incremental change dependency as follows:

$$m_{Rise} = \frac{v_{IN}}{L} = \frac{dI_L}{dt} \quad [21.7]$$

A small-signal  $v_{IN}$  results in a slope change with the same sign, but a decrease in the  $T_0$  to  $T_0 + DT_S$  interval equivalent to a decrease in duty cycle. We have seen that our example shows good line regulation and rejects sinusoidal variations in  $V_{IN}$  quite well. The

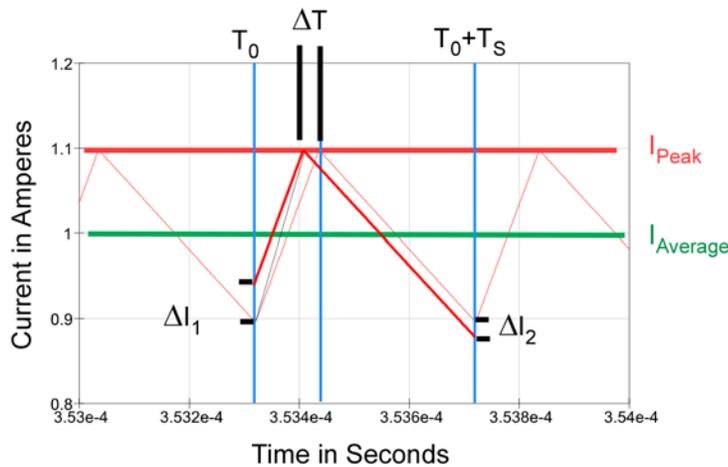


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excellent line rejection is a consequence of the operating point for the example as will become clear in the following.

For a quasi-static peak-to-peak ripple current, we show that in a single cycle:

$$m_{Rise} = \frac{I_{L-Peak-to-Peak}}{\Delta T} \quad [21.8]$$



**Figure 21.2 Current-Mode Control Incremental Equivalentents**

In figure 21.2, we see that an incremental increase in the  $m_{Rise}$  slope produces a  $\Delta T$  incremental decrease in the  $T_0 + DT_S$  interval, as well as a  $\Delta T$  incremental increase in the  $T_0 + DT_S$  to  $T_0 + T_S$  interval. If we interpret the increase in the  $m_{Rise}$  slope as an isolated event, the momentary event is equivalent to a single instantaneous incremental change  $\Delta I_1$  at the  $T_0$  event.

$$|M_{Rise}| = \left| \frac{\Delta I_1}{\Delta T} \right| \quad [21.9]$$

In a similar fashion, the  $\Delta T$  incremental increase in the  $T_0 + DT_S$  to  $T_0 + T_S$  interval produces an incremental current  $\Delta I_2$  at the  $T_0 + T_S$  event.

$$|M_{Fall}| = \left| \frac{\Delta I_2}{\Delta T} \right| \quad [21.10]$$

$$\left| \frac{M_{Rise}}{\Delta I_1} \right| = |\Delta T| = \left| \frac{M_{Fall}}{\Delta I_2} \right| \quad [21.11]$$



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$$\left| \frac{\Delta I_2}{\Delta I_1} \right| = \left| \frac{M_{Fall}}{M_{Rise}} \right| \quad [21.12]$$

Except for the difference in sign, the  $\Delta I_2$  at the  $T_0 + T_S$  event is similar to the single instantaneous incremental change  $\Delta I_1$  at the  $T_0$  event. The relationship between the slopes determines whether the incremental current magnitude is reduced or grows in following cycles.

We refer to figure 21.1 with a constant peak-to-peak ripple current to show:

$$DT_S M_{Rise} + (1-D)T_S M_{Fall} = 0 \quad [21.13]$$

$$DM_{Rise} = -(1-D)M_{Fall} \quad [21.14]$$

$$\frac{D}{1-D} = -\frac{M_{Fall}}{M_{Rise}} \quad [21.15]$$

$$\left| \frac{D}{1-D} \right| = \left| \frac{M_{Fall}}{M_{Rise}} \right| = \left| \frac{\Delta I_2}{\Delta I_1} \right| \quad [21.16]$$

After a number “N” of cycles, we have:

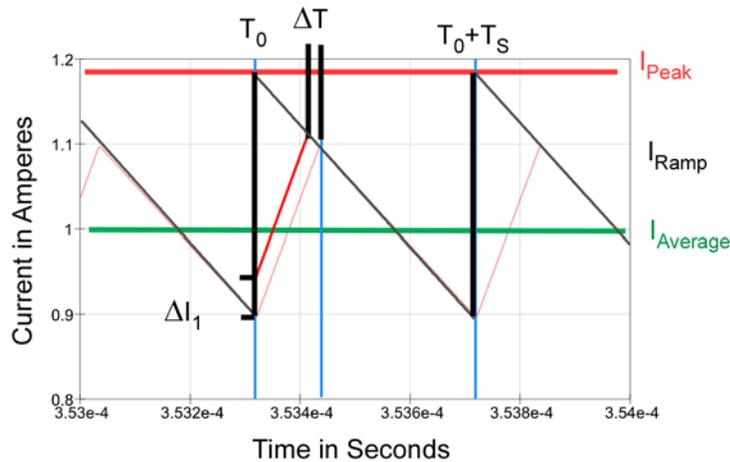
$$|\Delta I_N| = \left| \frac{D}{1-D} \right|^N |\Delta I_1| \quad [21.17]$$

We see that for  $D = 0.5$ , an incremental disturbance persists, and for  $D > 0.5$ , it grows without bound.

To remove the effects of disturbances, we add a periodic “Slope Compensation” sawtooth waveform to the  $I_{Peak}$  comparator reference signal as shown in figure 21.3 below:



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**Figure 21.3 Current-Mode Control with Slope Compensation Sawtooth**

With the addition of the sawtooth waveform, the  $I_{Peak}$  comparator level is initiated at a higher level and the periodic sawtooth “Slope Compensation” waveform is subtracted, decreasing the  $I_L$  peak intersection as shown. The disturbance current causes an intersection at a new time, produces a new incremental  $\Delta T$ , but because the periodic sawtooth “Slope Compensation” waveform is chosen with its slope identical to the  $M_{Fall}$  slope, there is no resulting  $\Delta I$  disturbance after the first cycle.

$$\Delta I_N = \left[ -\frac{M_{Fall} - M}{M_{Rise} + M} \right]^N \Delta I_1 \quad [21.18]$$

The parameters in equation [21.18] include the equivalent magnitudes of the slope of the compensation sawtooth  $M$ , as well as the  $I_L$  slopes. Magnitudes are used throughout to remove sign confusions arising from the rising and falling slopes.

**22.0 Summary and Conclusions**

We have introduced the Switchmode Buck converter that is used widely for high efficiency conversion of DC power available at a higher voltage and delivered to a load at a lower voltage. This course developed models of the Buck converter with current-mode control. We included basic operation, a practical set of examples, and large/small signal models were discussed. The considerations for feedback regulation and load-current limiting control of the converter were introduced.



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The selection of appropriate inductor and capacitor values were discussed, considering the frequency of operation and other design parameters. A constant-frequency Pulse-Width Modulator (PWM) controller is exemplified for pulse-by-pulse peak-current control. A method for constructive use of inductor parasitics was employed for current monitoring. We introduced the peak-threshold current control in the open-loop model to illustrate a current-limit function, and then developed that control into the pulse-by-pulse current-mode control for voltage feedback. We developed the feedback conditions for frequency-domain, small-signal, stability in the open-loop model and included a Pole-Zero (PZ) compensator for good margins. We introduced the Zero-Order-Hold (ZOH) effects of the inherent sampling caused by cycle-by-cycle control and included those effects in the (PZ) compensator. The loop was closed and a “soft-start” capability added to avoid current-limiting during startup. Line and load regulation was shown for the example as well as transient load recovery. Finally, the need for “Slope Compensation” in some designs was discussed and a means for adding it shown.

We have demonstrated that current-mode control of the Buck converter is an effective design approach to employ for this important switch-mode power converter.