A SunCam Online Continuing Education Course

Electronics

Course I Fundamentals
Course II Fundamental Devices—Parts I, II, III
Course III Miscellany Devices—Parts IV, V, VI

Miscellany Devices—Multivibrators / Phase Locked Loops / RTD / Ladder Logic

by

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Nomenclature[1]

A	constant	$K^{-8} \cdot m^{-8}$
A	gain	-
BW	bandwidth	Hz
C	capacitance	F
c, c	speed of light, $2.9979 \cdot 10^{8}$	m/s
$CMRR$	common-mode rejection ratio	-
D	diffusion constant	m^2 / s
E	energy	J or eV
E	source voltage	V
E, **E**	electric field strength	V/m
f	frequency	Hz
F_m	figure of merit	rad/s
G	gain	-
GBW	gain bandwidth	rad/s
h	Planck's constant, $6.6256 \cdot 10^{-34}$	$J \cdot s$
H	high	V
h_{fe}	CE small-signal (AC) forward current transfer ratio or gain	-
h_{FE}	CE small-signal (DC) forward current transfer ratio or gain	-
i	instantaneous or variable current	A
I, **I**	constant or rms current or effective or DC current	A
I_{CBO}	reverse saturation current	A
I_{EBO}	DC emitter cutoff current	A
I_{ZK}	keep-alive current	A
n	electron concentration [negative charge concentration]	cm^{-3}
n, N	concentration	m^{-3}
N	fan-out (number of loads)	-
p	hole concentration [positive charge concentration]	cm^{-3}
p	pole strength	Wb (N/T)
P	polarization	C/m^2
P	power	W
p^+	charge on a proton, $1.6022 \cdot 10^{-19}$	C
q	electric unit charge; charge of an electron, $-1.6022 \cdot 10^{-19}$	C
q, Q	charge, electric unit charge $1.6022 \cdot 10^{-19}$	C

[1] Not all the nomenclature, symbols, or subscripts may be used in this course—but they are related and may be found when reviewing the references listed for further information. Further, all the nomenclature, symbols, or subscripts will be found in of many electrical courses (on SunCam, PDH Academy, and also in many texts). For guidance on nomenclature, symbols, and electrical graphics: IEEE 280-2021, IEEE Standard Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering, New York: IEEE; and IEEE 315-1975, Graphic Symbols for Electrical and Electronics Diagrams, New York: IEEE, approved 1975, reaffirmed 1993.

r, R	resistance	Ω
S_R	slew rate	V/s
T	temperature	K
t	time	s
T	temperature	K
U	energy	J
υ or v	instantaneous or variable voltage	V
V	constant or rms voltage or effective or DC voltage	V
VR	voltage regulation	%
V_T	voltage equivalent of temperature	V
Z	impedance	Ω

Symbols

α	CB forward current ratio or gain	-
β	CE forward current ratio or gain	-
δ	feedback factor	-
ε	permittivity	F/m $\left(C^2 / N \cdot m^2\right)$
ε_0	permittivity of free-space, 8.854×10^{-12}	F/m $\left(C^2 / N \cdot m^2\right)$
κ	Boltzmann's constant, 1.3807×10^{-23}	J/K
μ	mobility	$m^2 / V \cdot s$
μ	permeability	H/m $\left(N / A^2\right)$
μ_0	free-space permeability, 1.2566×10^{-6}	H/m $\left(N / A^2\right)$
σ	conductivity	S/m
ω	angular frequency	rad/s

Subscripts

0	original, origin, zero value, at-rest value, evaluated value, at 0K, barrier value, resonance	-
A	acceptor	-
A,B	input A, input B	-
ac	ac current or small signal	=
amp	amplifier	-
ave	average	-
B	DC or biased base	-
b, B	base	-
BB	base supply or base biasing	-
be, BE	base to emitter	-
BO	breaker over	-
BQ	base or quiescent point	-
c	conduction band or AC or small-signal collector	-
C	collector	-
C	DC or biased collector	-
c, C	collector or control	-
CB	collector to base	-
CC	collector supply	-
CE	collector to emitter	-
cl	current limiting	-
cm	common mode	-
co, CO	cutoff	-
d	diffusion	-
D	donor, diode, or drain	-
d	delay	-
D	diode	-
DC	direct current	-
DD	drain supply	-
dm	differential mode	-
e	AC or small-signal emitter	-
E	DC or biased emitter	-
e,E	emitter	-
EBO	emitter to base, collector open	-
EE	emitter supply	-
f	forward (AC or instantaneous)	-
F	forward (DC component) or total	-
f	fall, feedback, or forward (AC or instantaneous)	-
F	forward (DC component or total)	-
fl	full load	-

G	gap or gate	-
GS	gate to source	-
H	hold	-
i	intrinsic or input (AC or instantaneous)	-
I, I	current	-
L	load	-
m	maximum	-
m	merit	-
max	maximum	-
min	minimum	-
n	electrons or *n*-type	-
n	noise	-
nl	no load	-
p	holes or *p*-type	-
p	power	-
pn	*p* to *n*	-
r	reverse (AC or instantaneous)	-
R	reverse (DC component or total)	-
r	rise	-
R	resistance	-
ref	reference	-
RTD	resistance temperature detector	-
s	saturation	-
S	source	-
t	transition	-
T	thermal	-
u	unity	-
υ, v, U	instantaneous voltage	-
v	valence band	-
V	constant or effective voltage	-
V	voltage	-
Z	zener	-
ZK	zener knee	-
ZM	zener at maximum rated current/voltage	-

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TABLE OF CONTENTS

Nomenclature....2
Symbols....3
Subscripts....4
List of Equations....8
COURSE INTRODUCTION....9
OVERVIEW & PERIODIC TABLE....9
PART IV SWITCHES, LOGIC TYPES....10
Transistor Switch Fundamentals....10
JFET Switches....12
CMOS Switches....13
Active Waveform Shaping....14
Logic Families....15
Logic Gates....16
Simplification of Binary Variables....16
Logic Circuit Fan-Out....18
Logic Circuit Delays....24
Resistor-Transistor Logic (RTL)....26
Diode-Transistor Logic (DTL)....26
Transistor-Transistor Logic (TTL or T^2L)....27
Emitter-Coupled Logic (ECL)....29
MOS Logic....30
CMOS Logic....31
PART V: MULTIVIBRATOR TYPES....33
Multivibrators....33
PART VI: CIRCUITS AND DEVICES....36
Circuit: Phase-Locked Loop (PLL)....36
Devices: RTDs and Resistant Bridges....38
Ladder Logic....40
Ladder Logic Timers....46
REFERENCES....48
Appendix A: Equivalent Units Of Derived And Common SI Units....49
Appendix B: Physical Constants....50
Appendix C: Fundamental Constants....52
Appendix D: Mathematical Constants, Signs/Symbols, Maxwell's Equations....53
Appendix E: The Greek Alphabet....54
Appendix F: SI Prefixes....54
Appendix G: Comparison of Electric & Magnetic Equations....55
Appendix H: Coordinate Systems and Related Operations....57

List of Figures

Figure 1: Periodic Table 9
Figure 18: Transistor Switch 11
Figure 19: JFET Switch 12
Figure 20: CMOS Inverter 13
Figure 21: CMOS Switch 14
Figure 22: NOT Gate 19
Figure 23: Fan-Out Unit Loads 19
Figure 24: Fan-Out Circuits 21
Figure 25: Load Lines 22
Figure 26: Logic Circuit Delays 25
Figure 27: Resistor-Transistor Logic 26
Figure 28: Diode-Transistor Logic 27
Figure 29: Transistor-Transistor Logic 28
Figure 30: Emitter-Coupled Logic 29
Figure 31: MOS Logic 30
Figure 32: CMOS Logic 32
Figure 33: Multivibrator Types 33
Figure 34: Multivibrator (Op Amp) Circuits 33
Figure 35: 555 Eight Pin Timer 34
Figure 36: 555 Timer Astable Multivibrator Internal Block Diagram 35
Figure 37: 555 Timer Astable Multivibrator Connections 35
Figure 38: 555 Timer Bistable Multivibrator Connections 35
Figure 39: 555 Timer Monostable Multivibrator 36
Figure 40: Phase-Locked Loop Functional Block Diagram 37
Figure 41: Voltage-Controlled Oscillator (VCO) Circuit 37
Figure 42: Two-Wire Resistance Bridge 38
Figure 43: Three-Wire Resistance Bridge 39
Figure 44: Ladder Logic with Standard Symbols 41
Figure 45: Ladder Logic with Timer 42
Figure 46: Ladder Logic with Nonstandard Symbols and Numbered Rungs 43
Figure 47: Ladder Logic for Standard Logic Gates 44
Figure 48: PLC and Ladder Logic Relationships 45
Figure 49: ON Delay Timer 46
Figure 50: OFF Delay Timer 47

List of Tables

TABLE 2: LOGIC GATES 16
TABLE 3: LOGIC FAMILY DATA 25

List of Equations

EQUATION 36: TRANSISTOR ON STATE—COLLECTOR CURRENT 10
EQUATION 37: SATURATION CONDITION—ON STATE—BASE CURRENT 11
EQUATION 38: UNIT SOURCE CURRENT 20
EQUATION 39: COLLECTOR CURRENT & UNIT SINK CURRENT 20
EQUATION 40: FAN-OUT MODEL EQUATION 21
EQUATION 41: LOAD LINE—SOURCING MULTIPLE LOADS 22
EQUATION 42: LOAD TRANSISTOR BASE CURRENT 22
EQUATION 43: SOURCING EQUATION—TRANSISTOR NOT GATE 22
EQUATION 44: SINK EQUATION—TRANSISTOR NOT GATE 23
EQUATION 45: SOURCE FAN-OUT 23
EQUATION 46: SINK FAN-OUT 23
EQUATION 47: RTD BALANCED 38

List of Examples

EXAMPLE 10 17
EXAMPLE 11 24
EXAMPLE 12 39
EXAMPLE 13 46

NOTE

The numbering scheme for figures and equations is a carryover from Electronics Course II.

A SunCam Online Continuing Education Course

COURSE INTRODUCTION

The theoretical information is primarily from the author's books, Refs. [A] and [B]. The NESC Ref. [C] and NEC Ref. [D] though not covered in this course are useful sources for electrical engineers. Information useful in many aspects of electric engineering may be found in [E] and [F]. Reference [G] has detailed descriptions of analysis techniques. Reference [H] covers many terms in EE with excellent definitions and explanations. The appendices cover information useful in many engineering tasks with App. G providing a side by side comparison of electric and magnetic equations. Use these texts or their counterparts for indepth information. References in bold are highly recommended.

This course will focus on basics, that rarely change, and provide the basis for all other knowledge.

OVERVIEW & PERIODIC TABLE

Electronics involves charge motion through materials other than metals, such as vacuums, gases, or semiconductors. The focus in this course will be on semiconductor materials. Because an understanding of the electron structure is vital to understanding electronics, a periodic table of the elements is shown below.

The Periodic Table of Elements (Long Form)

The number of electrons in filled shells is shown in the column at the extreme left; the remaining electrons for each element are shown immediately below the symbol for each element. Atomic numbers are enclosed in brackets. Atomic weights (rounded, based on carbon-12) are shown above the symbols. Atomic weight values in parentheses are those of the isotopes of longest half-life for certain radioactive elements whose atomic weights cannot be precisely quoted without knowledge of origin of the element.

periods	metals 1		transition metals 3	4	5	6	7	8	9	10	11	12	nonmetals 13	14	15	16	17	18
1 0	1.00794 H[1] 1	2																4.00260 He[2] 2
2 2	6.941 Li[3] 1	9.01218 Be[4] 2											10.811 B[5] 3	12.0107 C[6] 4	14.0067 N[7] 5	15.9994 O[8] 6	18.9984 F[9] 7	20.1797 Ne[10] 8
3 2,8	22.9898 Na[11] 1	24.3050 Mg[12] 2											26.9815 Al[13] 3	28.0855 Si[14] 4	30.9738 P[15] 5	32.065 S[16] 6	35.453 Cl[17] 7	39.948 Ar[18] 8
4 2,8	39.0983 K[19] 8,1	40.078 Ca[20] 8,2	44.9559 Sc[21] 9,2	47.867 Ti[22] 10,2	50.9415 V[23] 11,2	51.9961 Cr[24] 13,1	54.9380 Mn[25] 13,2	55.845 Fe[26] 14,2	58.9332 Co[27] 15,2	58.6934 Ni[28] 16,2	63.546 Cu[29] 18,1	65.38 Zn[30] 18,2	69.723 Ga[31] 18,3	72.64 Ge[32] 18,4	74.9216 As[33] 18,5	78.96 Se[34] 18,6	79.904 Br[35] 18,7	83.798 Kr[36] 18,8
5 2,8,18	85.4678 Rb[37] 8,1	87.62 Sr[38] 8,2	88.9059 Y[39] 9,2	91.224 Zr[40] 10,2	92.9064 Nb[41] 12,1	95.96 Mo[42] 13,1	(98) Tc[43] 14,1	101.07 Ru[44] 15,1	102.906 Rh[45] 16,1	106.42 Pd[46] 18	107.868 Ag[47] 18,1	112.411 Cd[48] 18,2	114.818 In[49] 18,3	118.710 Sn[50] 18,4	121.760 Sb[51] 18,5	127.60 Te[52] 18,6	126.904 I[53] 18,7	131.293 Xe[54] 18,8
6 2,8,18	132.906 Cs[55] 18,8,1	137.327 Ba[56] 18,8,2	* (57-71)	178.49 Hf[72] 32,10,2	180.948 Ta[73] 32,11,2	183.84 W[74] 32,12,2	186.207 Re[75] 32,13,2	190.23 Os[76] 32,14,2	192.217 Ir[77] 32,15,2	195.084 Pt[78] 32,17,1	196.967 Au[79] 32,18,1	200.59 Hg[80] 32,18,2	204.383 Tl[81] 32,18,3	207.2 Pb[82] 32,18,4	208.980 Bi[83] 32,18,5	(209) Po[84] 32,18,6	(210) At[85] 32,18,7	(222) Rn[86] 32,18,8
7 2,8,18,32	(223) Fr[87] 18,8,1	(226) Ra[88] 18,8,2	† (89-103)	(265) Rf[104] 32,10,2	(268) Db[105] 32,11,2	(271) Sg[106] 32,12,2	(272) Bh[107] 32,13,2	(270) Hs[108] 32,14,2	(276) Mt[109] 32,15,2	(281) Ds[110] 32,17,1	(280) Rg[111] 32,18,1	(285) Cn[112] 32,18,2	(286) Nh[113] 32,18,3	(289) Nh[114] 32,18,4	(290) Mc[115] 32,18,5	(293) Lv[116] 32,18,6	(294) Ts[117] 32,18,7	(294) Og[118] 32,18,8

*lathanide series	138.905 La[57] 18,9,2	140.116 Ce[58] 20,8,2	140.908 Pr[59] 21,8,2	144.242 Nd[60] 22,8,2	(145) Pm[61] 23,8,2	150.36 Sm[62] 24,8,2	151.964 Eu[63] 25,8,2	157.25 Gd[64] 25,9,2	158.925 Tb[65] 27,8,2	162.500 Dy[66] 28,8,2	164.930 Ho[67] 29,8,2	167.259 Er[68] 30,8,2	168.934 Tm[69] 31,8,2	173.054 Yb[70] 32,8,2	174.967 Lu[71] 32,9,2
†actinide series	(227) Ac[89] 18,9,2	232.038 Th[90] 18,10,2	231.036 Pa[91] 20,9,2	238.029 U[92] 21,9,2	(237) Np[93] 23,8,2	(244) Pu[94] 24,8,2	(243) Am[95] 25,8,2	(247) Cm[96] 25,9,2	(247) Bk[97] 26,9,2	(251) Cf[98] 28,8,2	(252) Es[99] 29,8,2	(257) Fm[100] 30,8,2	(258) Md[101] 31,8,2	(259) No[102] 32,8,2	(262) Lr[103] 32,9,2

Figure 1: Periodic Table

NOTE

The numbering scheme for figures and equations is a carryover from Electronics Course II.

PART IV SWITCHES, LOGIC TYPES

Transistor Switch Fundamentals

The bipolar junction transistor (BJT) is an active nonlinear device that, when used between its saturation and cutoff regions, becomes an electronic switch. A transistor circuit set up to operate as a switch is shown in Fig. 18(a). The pulse input that controls the switch is shown in Fig. 18(b). The pulses can be considered to represent logic conditions.[2] Combinations of such switches can be used to build logic circuits. The characteristics of the switch, the two operating points, and approximate models are shown in Fig. 18(c).

When the transistor switch is in the on state, that is, saturated, the collector current is given by KVL in the output loop as

Equation 1: Transistor ON State—Collector Current

$$I_{C,\text{sat}} = \frac{V_{CC} - V_{CE,\text{sat}}}{R_L}$$

[2] Normally the logic conditions are voltage inputs. For transistor-transistor-logic (TTL) circuits, 0.0 V to 0.8 V is logic 0 and approximately 3.0 V is logic 1.

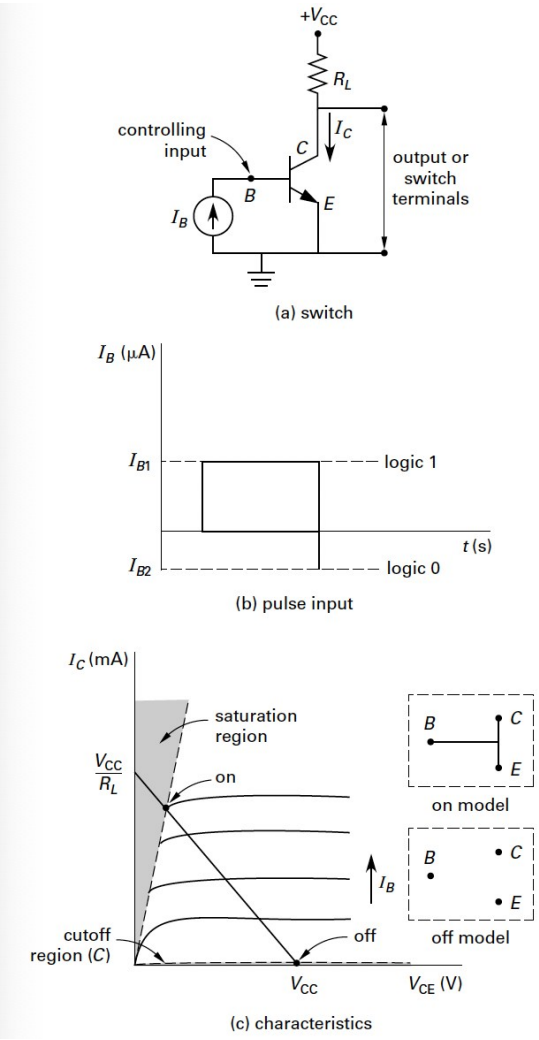


Figure 2: Transistor Switch

The collector-emitter voltage, V_{CE}, is typically 0.1 V for germanium diodes and 0.2 V for silicon diodes and can be ignored for first-order calculations—hence the short-circuit model of Fig. 18(c). The value of the load resistance must be determined so that when in saturation the condition of Eq. 37 is satisfied.[3]

Equation 2: Saturation Condition—ON State—Base Current

$$I_{B1} \square \frac{I_{C,\text{sat}}}{h_{\text{FE}}} \square \frac{V_{\text{CC}}}{h_{\text{FE}} R_L}$$

[3] At low frequencies, $h_{\text{FE}} \approx h_{\text{fe}}$, as is the case for all of the small-signal parameters. Reference [H] contains a list of electronic parameter meanings.

The base current calculated by Eq. 37 is the minimum current required to drive the transistor into saturation, ignoring the small collector-emitter voltage. When the transistor is in *saturation* (*on*), the base-emitter and collector-base junctions are both forward biased. When the transistor is in *cutoff* (*off*), the base-emitter and collector-base junctions are both reverse biased.

Field-effect transistors (FETs) are also used as switches. The gate provides the controlling input. In the ON condition, unlike the BJT, the properties of the FET are more like that of a resistor. In the OFF condition, small leakage currents flow, similar to reverse saturation currents in the BJT.

JFET Switches

Junction field-effect transistors used as switches are constructed from depletion-mode *p*-channel types as shown in Fig. 19.

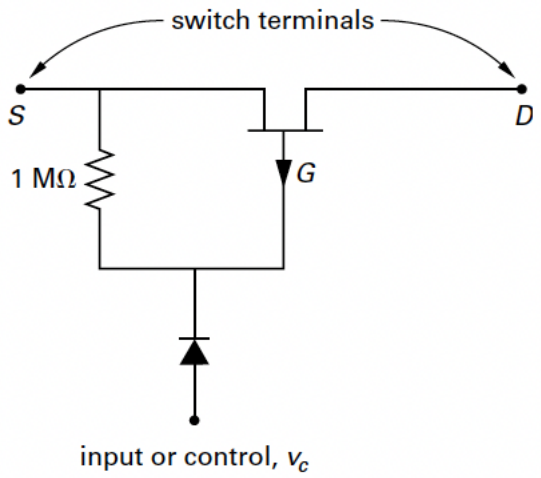


Figure 3: JFET Switch

When the control voltage, v_c, is zero, the gate-source voltage, V_{GS}, is equal to zero and the switch is ON. This occurs because the gate-channel *pn* junction controls the transistor by varying the depletion region caused by reverse bias. A positive control voltage results in a positive gate-source voltage, turning the switch OFF. This positive voltage is the pinchoff voltage, V_{GS}(off). The diode prevents forward bias (i.e., negative voltage) on the gate-channel pn junction, which would destroy the switching characteristics of the JFET.[4]

[4] The current from the gate would add to that flowing from source to drain. The device would no longer function strictly as a switch controlling external current.

The advantage of the JFET is its low resistance while in the on condition. Disadvantages include complexity and price. Further, the JFET is restricted to switching voltages a few volts less than the control voltages, because anything larger could turn the switch on. Also, if the switching voltage becomes too large while in the on condition, the switch can turn off. That is, the JFET moves from the ohmic region to the pinchoff region (see Ref. [A] or [B]).

CMOS Switches

When a *p*-channel MOS device and an *n*-channel MOS device are fabricated on the same chip, the device is called a *complementary MOSFET* (CMOS).[5] A CMOS device used as an *inverter* or *digital switch* is illustrated in Fig. 20 along with the approximate output characteristics.

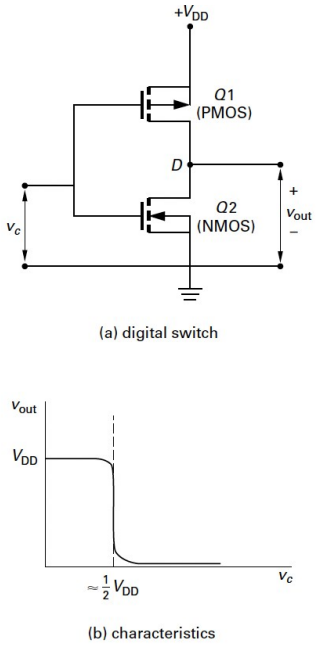


Figure 4: CMOS Inverter

The control or input voltage, v_c, varies from 0 V (logic 0) to $+V_{DD}$ (logic 1). When the control voltage is 0 V, the gate-source voltage of Q1 is negative and Q1 is ON. (The negative voltage attracts holes, enhancing the channel and allowing current flow.) The gate-source voltage of Q2 is zero and Q2 is OFF. (A positive voltage is required to attract electrons into the channel.) Consequently, Q1 can be modeled as a short circuit from source to drain, resulting in $v_{out} = +V_{DD}$ (logic 1). When the control voltage is $+V_{DD}$, the gate-source voltage of Q1 is zero and Q1 is OFF. The gate-source voltage of Q2 is positive and Q2 is ON. Consequently, Q2 can be modeled as a

[5] The design of such circuits is known as *static CMOS implementation*.

short circuit from source to drain, resulting in v_{out} = 0 V (logic 0). Current flows only during the switching transient. *The static current flow and static power are zero, so the power requirements of CMOS circuits are extremely low*.

An analog switch is created when the inverter is combined with a second CMOS device as shown in Fig. 21.

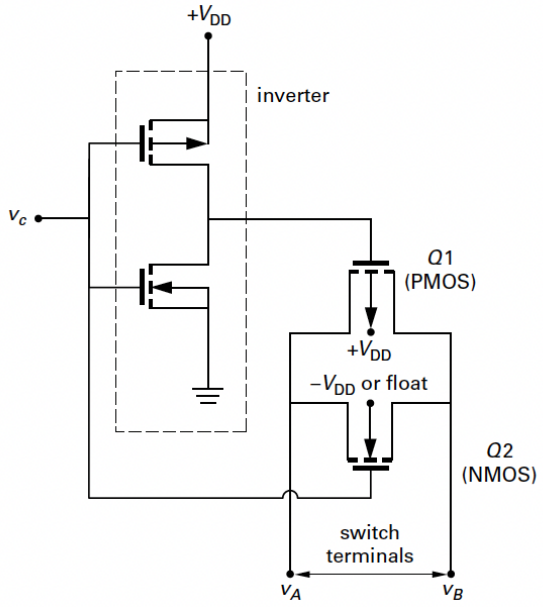


Figure 5: CMOS Switch

When the control voltage, v_c, is 0 V, both parallel switch channels (Q1 and Q2) are off. Q1 is OFF because $+V_{DD}$ is applied to its gate by the inverter. Q2 is OFF because 0 V is applied to its gate by the control voltage. In the off condition, restrictions on the switching terminals' voltage exist. For instance, Q1 will turn ON if both terminals are more positive than $+V_{DD}$ —hence the upper limit on the voltage. Q2 will turn ON if both terminals are negative by an amount equal to V_{GS}—hence a lower limit on the voltage. When the control voltage, v_c, is $+V_{DD}$, Q1 will turn ON when the switching voltage is positive enough to make V_{GS} negative enough to create the p-channel. Q2 will turn ON when the switching voltage is negative or within a few volts of V_{DD}.

Active Waveform Shaping

Waveform shaping occurs in many circuits using nonlinear active devices, with and without storage elements (capacitors and inductors). These devices can be discrete or integrated, although integrated circuits rely primarily on capacitors rather than inductors. No single simple theory describes the behavior of all these elements. The analysis is generally done by breaking the circuit into a sequence of linear problems and combining the results.

Examples of such circuits include operational amplifiers with capacitors and inductors (integrators and differentiators, filters), waveform generators (sweep, square, triangular), oscillator circuits (monostable, bistable, astable), and so on.

Logic Families

Integrated circuits are classified into families based on the circuit elements they contain and the manner in which these elements are combined. *Passive logic circuits* have no transistors (i.e., they have only resistors and diodes), while *active logic circuits* do have transistors.

One of the earliest logic families is *diode-transistor logic* (DTL). *High-threshold logic* (HTL) is similar to DTL but uses higher voltages and better diodes to produce greater noise immunity. *Variable-threshold logic* (VTL) is a variation of DTL with adjustable noise immunity. *Direct-coupled transistor logic* (DCTL) is an unsophisticated connection of transistors with poor immunity to noise and low logic levels. Because there are no resistors, it has low power dissipation. *Resistor-transistor logic* (RTL) is similar to DCTL with the addition of resistors to limit current hogging. *Resistor-capacitor transistor logic* (RCTL) is a low-cost compromise between speed and power. *Transistor-transistor logic* (TTL or T2L) is the fastest of all logic families using transistors operating in the saturated region. The fastest of all logic families using bipolar junction transistors is *emitter-coupled logic* (ECL), also known as *current-mode logic* (CML). ECL transistors do not operate in the saturation region. ECL circuits consume more power than TTL.

Metal-oxide semiconductor (MOS) circuitry contains MOSFETs. It requires few resistors and has high packing density. *Complementary construction* uses both *n*-channel and *p*-channel transistors in the same circuit. NMOS logic uses *n*-channel MOSFETs, while PMOS uses *p*-channel MOSFETs. (NMOS is approximately six times slower than PMOS.) *Complementary metal-oxide semiconductor* (CMOS), also known as *complementary transistor logic* (CTL), circuits have high packing density and reliability. They are capable of higher switching speeds than MOS.

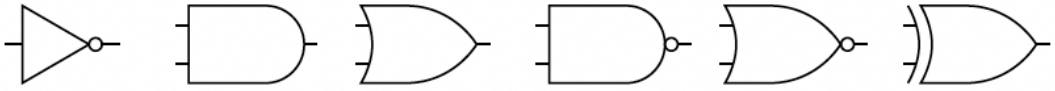
Circuitry based on bipolar transistors switches faster, offers greater current drive, and is more suitable for analog applications than CMOS circuitry.[6] On the other hand, CMOS consumes less power, dissipates less heat, and has a higher packing density. Bipolar and CMOS circuitry are combined in biCMOS integrated circuits.

[6] CMOS is equivalent to TTL in speed but slower than ECL.

Logic Gates

A *gate* performs a logical operation on one or more inputs. The inputs (labeled A, B, C, etc.) and output are limited to the values of zero or one. A listing of the output value for all possible input values is known as a truth table. Table 2 combines the symbols, names, and truth tables for the most common gates.

Table 1: Logic Gates



inputs		not	and	or	nand	nor	exclusive or
A	B	$-A$ or $\overline{A}$	AB	$A+B$	$\overline{AB}$	$\overline{A+B}$	$A \oplus B$
0	0	1	0	0	1	1	0
0	1	1	0	1	1	0	1
1	0	0	0	1	1	0	1
1	1	0	1	1	0	0	0

Simplification of Binary Variables

The rules of Boolean algebra are used to write and simplify expressions of binary variables (i.e., variables constrained to two values). The basic laws governing Boolean variables are as follows.

- *commutative*: $A + B = B + A$, $A \cdot B = B \cdot A$
- *associative*: $A + (B + C) = (A + B) + C$, $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- *distributive*: $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$, $A + (B \cdot C) = (A + B) \cdot (A + C)$
- *absorptive*: $A + (A \cdot B) = A$, $A \cdot (A + B) = A$

De Morgan's theorems are as follows.

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

The following basic identities are used to simplify Boolean expressions.

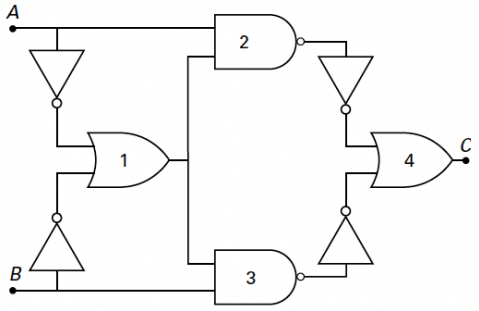
$$\begin{array}{lll} 0+0=0 & 0\cdot 0=0 & A+0 = A \\ 0+1=1 & 0\cdot 1=0 & A+1 = 1 \\ 1+0=1 & 1\cdot 0=0 & A+A = A \\ 1+1=1 & 1\cdot 1=1 & A+\overline{A} = 1 \end{array}$$

$$\begin{array}{ll} A\cdot 0 = 0 & -0=1 \\ A\cdot 1 = A & -1=0 \\ A\cdot A = A & -\overline{A} = A \\ A\cdot \overline{A} = 0 & \end{array}$$

Switching algebra is a form of Boolean algebra (see Ref. [A] and Ref. [B]).

Example 1

Simplify and write the truth table tables for the following network of logic gates.



Solution

Determine the inputs and output of each gate in turn.

gate	inputs	output
1	$\overline{A}, \overline{B}$	$(\overline{A}+\overline{B})$
2	$A, (\overline{A}+\overline{B})$	$\overline{A\cdot(\overline{A}+\overline{B})}$
3	$B, (\overline{A}+\overline{B})$	$\overline{B\cdot(\overline{A}+\overline{B})}$
4	$A\cdot(\overline{A}+\overline{B}),$ $B\cdot(\overline{A}+\overline{B})$	$A\cdot(\overline{A}+\overline{B})$ $+B\cdot(\overline{A}+\overline{B})$

Simplify the output of gate 4.

$$
\begin{aligned}
&A \cdot (\overline{A} + \overline{B}) + B \cdot (\overline{A} + \overline{B}) && \text{[original]}\\
&A \cdot \overline{A} + A \cdot \overline{B} + B \cdot \overline{A} + B \cdot \overline{B} && \text{[distributive]}\\
&A \cdot \overline{B} + B \cdot \overline{A} && \text{[since } A \cdot \overline{A} = 0\text{]}\\
&A \bigoplus B && \text{[definition]}
\end{aligned}
$$

The resulting truth table follows.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Logic Circuit Fan-Out

Fan-out is the number of parallel loads that can be driven from one output node of a logic circuit. Because logic circuits are routinely cascaded in order to achieve the desired outcome, a single transistor's output must provide multiple inputs for subsequent stages.

Consider the NOT gate shown in Fig. 22, which is a common emitter-configured transistor with the output taken from the collector. The transistor is designed to operate as a switch between the saturation and cutoff regions. When the input is high (several volts), the base-emitter junction is forward biased and the base current is sufficient to saturate the transistor. The output is then low, nearly zero if the small collector-emitter voltage (0.2 V for silicon transistors and 0.1 V for germanium) is ignored. The input has been inverted, that is, changed from high to low—hence the designation as a NOT gate.[7]

[7] The logic described here and used throughout this course is positive logic, that is, logic where the high voltage is logic condition 1 and the low voltage is logic condition 0. Negative logic is the reverse. Dynamic or pulse logic is a system where the presence of a pulse is logic condition 1 and the absence of a pulse is logic condition 0.

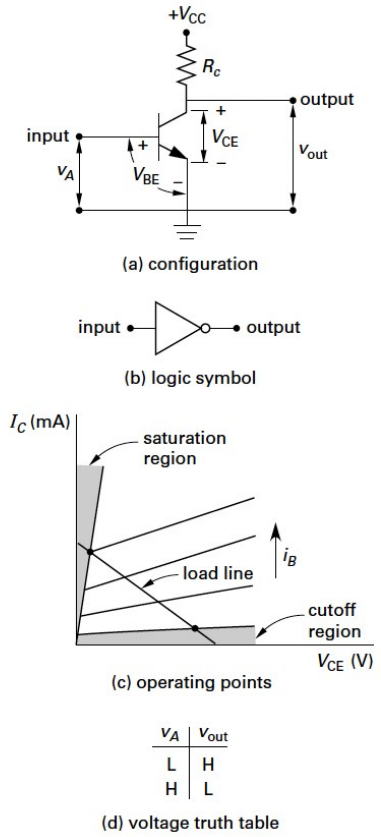


Figure 6: NOT Gate

In practical applications, this transistor does not operate in isolation, but instead is cascaded with other logic devices. The base current drawn while in saturation is sourced from previous stages. When in cutoff, the reverse saturation current, I_{CBO}, flowing through the collector-base junction must be sunk by previous stages. This situation is shown in Fig. 23.

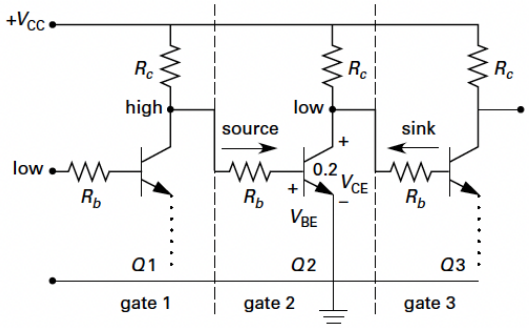


Figure 7: Fan-Out Unit Loads

The number of stages a logic gate can source, that is, the current a stage can supply when its collector voltage is high, is called the *fan-out*. In Fig. 23, transistor Q1 is sourcing the current to Q2. The number of stages that a logic gate can sink, that is, the current the collector (or output circuit) can accept without removing the transistor from the saturated state, is also called the *fan-out*. In Fig. 23, transistor Q2 is sinking the current from Q3. A given logic family's fan-out specification is stated in terms of *unit loads*. A *unit source current* is the input current drawn by a single gate when the voltage is high. A unit sink current is the current drawn from the input of a single gate when the input voltage is low. The fan-out specification is the minimum number of unit loads, source or sink, the gate can provide.

Gate 1 in Fig. 23 sources a unit load to Q2. Q1 is cut off and appears as an open circuit.[8] The unit source current is the base current to Q2 given by Gate 1 in Fig. 23 sources a unit load to Q2. Q1 is cut off and appears as an open circuit. The unit source current is the base current to Q2 given by

Equation 3: Unit Source Current

$$I_{B2} = \frac{V_{CC} - V_{BE2}}{R_c + R_b}$$

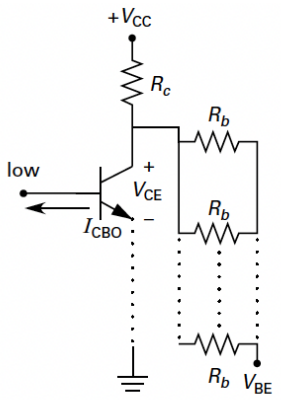
Q2 is saturated, which causes Q3 to be cut off. The reverse saturation current, I_{CBO}, from the collector-base junction of Q3 is drawn to the collector of Q2. (This sink current raises the voltage at the collector of Q2. If too much current is drawn, the voltage rise can reverse-bias the collector-base junction of Q2, bringing it out of saturation.) The unit sink current is I_{CBO3}. The collector current is

Equation 4: Collector Current & Unit Sink Current

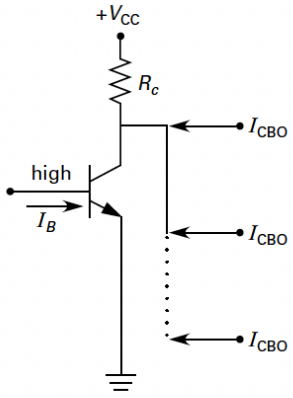
$$I_{C2} = \frac{V_{CC} - V_{CE,sat}}{R_c} + I_{CBO3}$$

When a gate's function is to maintain multiple loads, the source and sink transistors can be modeled as shown in Fig. 24 in order to determine the fan-out.

[8] Because the threshold voltage is approximately 0.7 V for a silicon base-emitter junction, Q1 will be cut off at voltages of 0.6 V or less.



(a) source loads



(b) sink loads

Figure 8: Fan-Out Circuits

For the sourcing condition of Fig. 24(a), applying KCL at the collector node gives

Equation 5: Fan-Out Model Equation

$$\frac{V_{CC}-V_{CE}}{R_c}-I=N\left(\frac{V_{CC}-V_{CE}}{R_b}\right)$$

The forward base-emitter voltage required to hold the load transistors in saturation is typically ≈ 0.7 V, and the reverse saturation is I_{CBO}. The current in the collector resistor, R_c, includes the reverse saturation current, I_{CBO}, of the cutoff transistor.[9]

[9] The collector current is not shown in Eq. 40 as the reverse saturation current because this equation is used in a general manner to determine the load line.

The load line equation without sourced loads is shown as a dashed line in Fig. 25(a).

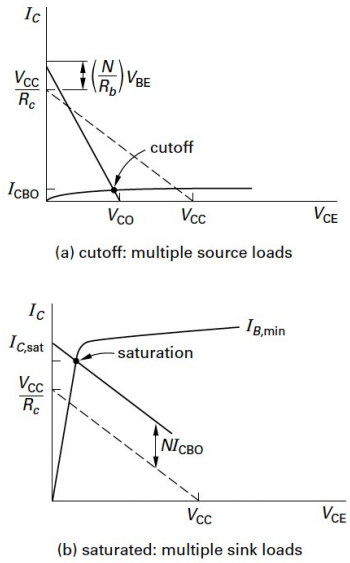


Figure 9: Load Lines

The load line for a transistor sourcing multiple loads is shown as a solid line in Fig. 25(a) and is given by Eq. 37.40 rearranged as

Equation 6: Load Line—Sourcing Multiple Loads

$$I_C + \left(\frac{1}{R_c} + \frac{N}{R_B}\right)V_{CE} = \frac{V_{CC}}{R_c} + \left(\frac{N}{R_b}\right)V_{BE}$$

Each load transistor has a base current given by the following.

Equation 7: Load Transistor Base Current

$$I_B = \frac{V_{CE} - V_{BE}}{R_b}$$

Substituting the restriction of Eq. 42 into the load line equation, Eq. 41, gives the sourcing equation for this type of logic gate.

Equation 8: Sourcing Equation—Transistor NOT Gate

$$I_C + \left(N + \frac{R_b}{R_c}\right)I_B = \frac{V_{CC} - V_{CE}}{R_c}$$

For the sink condition of Fig. 24(b), applying KCL at the collector node gives

Equation 9: Sink Equation—Transistor NOT Gate

$$I_{C,\text{sat}} = \frac{V_{\text{CC}} - V_{\text{CE,sat}}}{R_c} + NI_{\text{CBO}}$$

The load lines for the sink condition are taken directly from Eq. 37.44 and are shown in Fig. 25(b). Once the minimum collector saturation current is determined by Eq. 44 for the sink condition, which depends on the sink fan-out (N), the minimum base current required to maintain the transistor in saturation can be graphically determined from the characteristic curve as shown in Fig. 25(b). The base current curve that exists at the point where the load line curve for multiple sinking loads intersects the calculated collector saturated current determines the minimum base current.[10]

Once the equations for the source condition, Eq. 43, and sink condition, Eq. 44, are determined, the collector current, I_C, is set as the reverse saturation current, I_{CBO}, in the source equation and both equations are solved for the fan-out, N. The *source fan-out* is

Equation 10: Source Fan-Out

$$N + \frac{R_b}{R_c} \leq \frac{V_{\text{CC}} - V_{\text{BE}} - I_{\text{CBO}}R_c}{I_{B,\text{min}}R_c}$$

The *sink fan-out* is

Equation 11: Sink Fan-Out

$$N \leq \frac{I_{C,\text{sat}}R_c + V_{\text{CE,sat}} - V_{\text{CC}}}{I_{\text{CBO}}R_c}$$

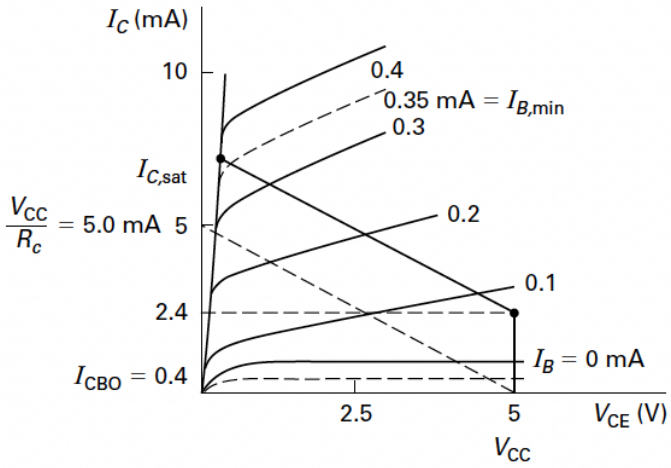
The procedure for determining the fan-out for other types of logic is similar.

---

[10] The minimum base current, $I_{B,\text{min}}$, is the base current that a sourcing gate must supply as well as the minimum base current it requires when operating in the sink condition.

Example 2

Given a transistor with the characteristic shown, $R_c = 1000\ \Omega$ and $V_{CC} = 5$ V, determine the base current necessary for a fan-out of five.



Solution

Because I_{CBO} = 0.4 mA, five load gates require 5 × 0.4 mA = 2 mA excess current. The corresponding load line is shown solid. The resulting saturation current requires a base current of about 0.35 mA. (Setting the value at 0.4 mA gives a margin of error for temperature effects and variations between transistors.)

Logic Circuit Delays

Logic circuits do not switch instantly from cutoff to saturation, or vice versa, upon application of an input pulse. Various delays are inherent, as shown in Fig. 26.

When the input voltage level (pulse) rises, a finite time, called the delay time, t_d, is required for the base-emitter junction of the transistor in the inverter circuit to reach the turn-on level. The time for the input voltage to rise enough for the collector output voltage to fall to the saturation level is called the rise time, t_r.

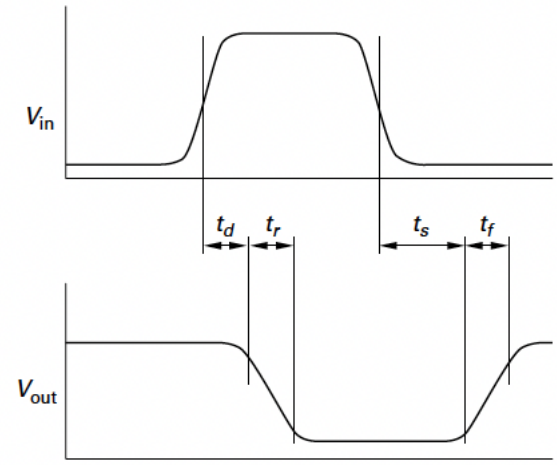


Figure 10: Logic Circuit Delays

With the transistor in saturation, both the base-emitter and collector-base junctions are forward biased. Excess charge is stored in the base region, that is, the spacecharge region is small. When the input voltage level (pulse) drops, a finite time is required to remove the excess charges in the base. This delay is called the storage time, t_s. Once the excess charge is removed, the collector current falls. This time is called the fall time, t_f.

The minimum time for a transistor to pass a pulse, that is, the time from cutoff to saturation and back to cutoff, or vice versa, is the sum of all the delays. *The maximum frequency at which a transistor can operate is the reciprocal of the sum of these delays.*

The sum of the delays is called the propagation delay for a given logic gate. Approximate fan-out and propagation delay values for various transistor logic families, listed left to right in the approximate order of development, are given in Table 3.[11]

Table 2: Logic Family Data

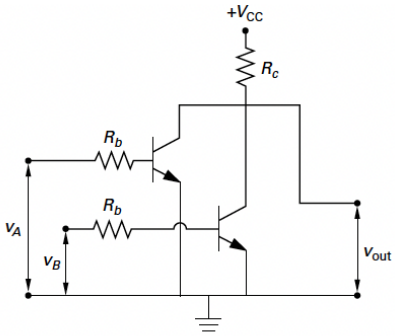
parameter	RTL	DTL	HTL	TTL	ECL	MOS	CMOS
basic gate[a]	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR OR NAND
fan-out[b]	5	8	10	10	25	20	> 50
propagation delay[c]	12	30	90	10	0.1	10	0.1

[a]Positive logic is assumed when determining the basic gate.
[b]Worst-case condition.
[c]Approximate values in nanoseconds.

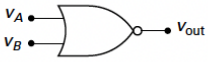
[11] One method of designing to handle such delays is by using clocked logic , that is, logic controlled by a clock so that the flow of signals follows a known parameter.

Resistor-Transistor Logic (RTL)

The basic gate of the resistor-transistor logic (RTL) family is the NOR gate as shown in Fig. 27. The inverter used to describe fan-out is the basic building block. Although a *fan-in* of two is shown in Fig. 27, multiple inputs are possible. Logic 1 (high voltage) at any input saturates the associated transistor, causing the output to be connected to ground across the small collector-emitter voltage, resulting in a logic 0 (low voltage) output.



(a) basic gate: NOR



(b) logic symbol

v_A	v_B	v_{out}
L	L	H
L	H	L
H	L	L
H	H	L

(c) voltage truth table

Figure 11: Resistor-Transistor Logic

Diode-Transistor Logic (DTL)

The basic gate of the diode-transistor logic (DTL) family is the NAND gate shown in Fig. 28. A fan-in of two is shown, but multiple inputs are possible. When either input is logic 0 (low voltage), the associated diode, *D*, conducts, resulting in a low voltage at node B. The base current to the transistor will be logic 0 because any current flow is blocked by diodes D1 and D2. (Two diodes are used to ensure that the transistor will not turn on with one input low.) The transistor is cut off, and the output is high (+VCC, logic 1). When both inputs are logic 1 (high voltage), neither of the diodes conduct and the voltage at node B rises toward $+V_{CC}$. Diodes D1 and D2 conduct, and the transistor saturates, causing V_{out} to be low ($V_{CE} \approx 0$ V, logic 0).

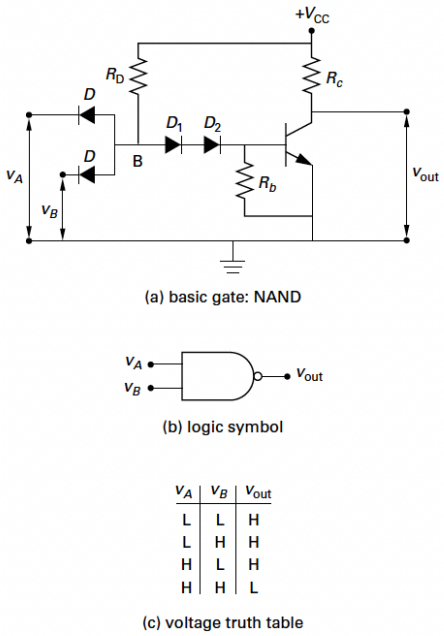
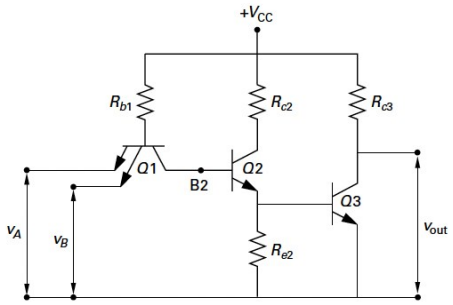


Figure 12: Diode-Transistor Logic

DTL uses less current than RTL when sourcing loads, but more current when sinking loads. Zero current is required to source a load using DTL logic because of the diodes. *High-threshold logic* (HTL) is similar but uses higher voltages and better diodes to improve noise performance.

Transistor-Transistor Logic (TTL or T²L)

The basic gate of the transistor-transistor logic (TTL) family is the NAND gate as shown in Fig. 29. The basic TTL NAND gate can be considered a modification of the DTL NAND gate. That is, the input diodes have been replaced by a multi-emitter transistor's base-emitter junctions. A fan-in of two is shown, but multiple inputs are possible. When at least one input is logic 0 (low voltage), the emitter of Q1 is forward biased. Assuming Q2 is cut off, the current supplied to the collector of Q1 is the reverse saturation current, IEBO, of the emitter-base junction of Q2. Because this current is small, $I_{B1} > I_{EBO}/h_{FE}$ and Q1 is in saturation. The voltage at node B2 is then equal to the input voltage, v_A or v_B, summed with $V_{CE,sat}$, that is, about 0.4 V to 0.8 V. This voltage is not enough to forward bias Q2 and Q3, because about 0.7 V apiece is required. Q3 is cut off, and the output is high (+VCC, logic 1). When all the inputs are at logic 1 (high voltage), the emitter-base junction of Q1 is reverse biased. Q1 is cut off and the base-collector junction is forward biased by approximately $+V_{CC}$. This voltage is high enough to forward bias the base-collector junction of Q1 and the base-emitter junctions of Q2 and Q3, about 2.1 V. So, the output is low ($V_{CE3} \approx 0$ V, logic 0).



(a) basic gate: NAND

(b) logic symbol

v_A	v_B	v_{out}
L	L	H
H	L	H
L	H	H
H	H	L

(c) voltage truth table

Figure 13: Transistor-Transistor Logic

TTL logic is the fastest-saturating logic gate. The fall time of TTL circuits is improved by reducing the collector current in the saturated state. This is accomplished by using a *totem-pole configuration*, also called *active pull-up*, which uses an additional transistor and diode in series with R_{c3}.[12] Additionally, the collector of Q3 can be left open, in which case it is called the *open-collector TTL gate*. The open-collector TTL gate is used with *wired logic* or *collector logic*, because the collector outputs are wired to the next gate's output without intervening circuitry. This allows the logic voltage level to be changed. For example, in Fig. 29, the driving voltage is $+V_{CC}$. If the collector of Q3 is open, that is, not connected to $+V_{CC}$ via R_{c3}, then a power source can be attached to the collector of Q3, providing a different voltage logic, say V_{CC}. (One can connect a +5 V logic circuit to a +12 V logic circuit without damaging the components.)

A type of logic with operational similarities to the open-collector logic is *tri-state logic*. In this case, the output of the transistor can be logic level 0, level 1, or level Z. The Z-level is a high-impedance level at which the output is completely disconnected from the rest of the circuit. This is accomplished by adding an enable (inhibit) circuit to the output, similar to the circuit used on clocked flip-flops to control sequencing. The high impedance level allows multiple circuits to connect to the same output line or bus so that several circuits can timeshare a bus. Only the active

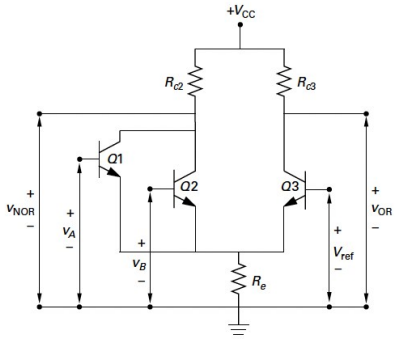
[12] This configuration is called the totem pole because the additional transistor sits on top of Q3.

circuit controls the bus. The others are in the Z-level state and have no impact on the voltage level, or signal, on the bus. Circuits with this tri-state logic are called *tri-state buffers*.

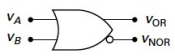
Emitter-Coupled Logic (ECL)

The basic gate of the emitter-coupled logic (ECL) family is the OR-NOR gate shown in Fig. 37. The basic building block of the family is the difference amplifier (Q2 and Q3 in Fig. 37.30). The transistors in this logic family do not saturate. Instead, they remain in the active region as the input voltages, v_A and v_B, operating above and below (logic 1 and logic 0) the reference voltage, V_{ref}. Because the emitter current through R_e remains approximately constant, when both inputs are logic 0 (i.e., below the reference voltage) the emitter currents from Q1 and Q2 are minimal and the emitter current of Q3 is maximum. This causes the voltage output at v_{OR} to be low (logic 0) and the voltage output at v_{NOR} to be high (logic 1). When either or both of the inputs are logic 1 (i.e., above the reference voltage) the emitter currents of Q1 and Q2 are maximum, and the emitter current of Q3 is minimal. This causes the voltage output at v_{OR} to be high (logic 1), and the voltage output at v_{NOR} to be low (logic 0).

ECL improves on the propagation delay of TTL by not driving the transistors into saturation. This minimizes the switching time, because charge carriers do not have to be cleared from the base junction. However, the power requirements of ECL are greater than TTL (see Table 2). Emitter-coupled logic is also called current mode logic (CML).



(a) basic gate: OR–NOR



(b) logic symbol

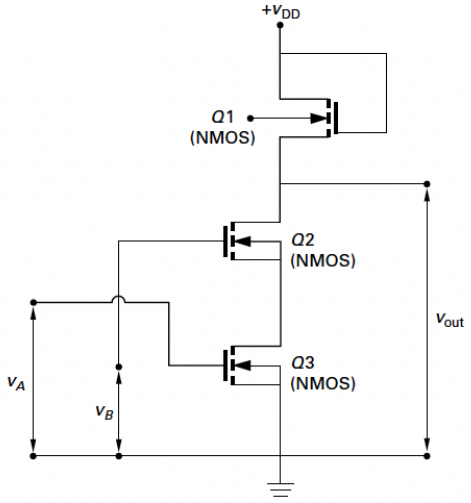
v_A	v_B	v_{OR}	v_{NOR}
L	L	L	H
H	L	H	L
L	H	H	L
H	H	H	L

(c) voltage truth table

Figure 14: Emitter-Coupled Logic

MOS Logic

The basic gate of the MOS logic family is the NAND gate as shown in Fig. 31. [13]The basic building block of the family is the inverter (Q1 and Q2 in Fig. 31). A fan-in of two is shown, but multiple inputs are possible. Q1 is always biased on by the drain power supply, $+V_{DD}$. When either input is logic 0 (low voltage), the associated transistor, Q2 or Q3, is off. No current flows and v_{out} is high ($+V_{DD}$, logic 1). When both of the inputs are logic 1 (high voltage), both transistors are on. Current flows and the output voltage is low ($v_{out} \approx 0$ V, logic 0).



(a) basic gate: NAND

(b) logic symbol

v_A	v_B	v_{out}
L	L	H
L	H	H
H	L	H
H	H	L

(c) voltage truth table

Figure 15: MOS Logic

MOS logic is simple and requires no external resistors or capacitors, making it well suited for realization in integrated circuit form. The NMOS positive logic shown in Fig. 31(a) draws power

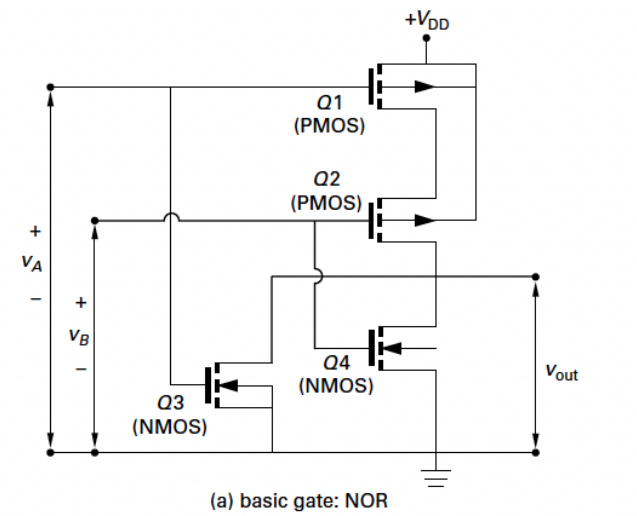
[13] This is the basic gate for positive logic NMOS. For positive logic PMOS, the basic gate is the NOR gate.

in only one state. The PMOS positive logic (NOR) draws power in three states. In both cases, the power drawn is less than for other logic families, allowing much higher device densities. NMOS is faster, because electron mobility is higher than hole mobility. PMOS is less expensive. Advances have made the propagation delays comparable to those for other logic families (see Table 2).

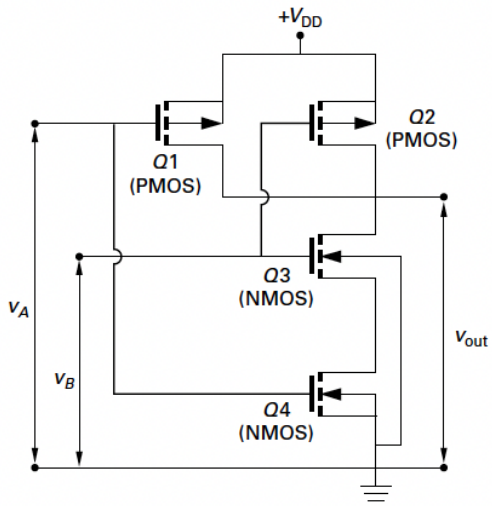
CMOS Logic

The basic gate of the CMOS logic family may be either the NOR gate or the NAND gate shown in Fig. 32. (Both are positive logic gates.) A fan-in of two is shown, but multiple inputs are possible. For the NOR gate in Fig. 32(a), when both of the inputs are logic 0 (voltage low), Q1 and Q2 are on, and Q3 and Q4 are off. The output is caused to be high ($\approx +V_{DD}$, logic 1) by the connection to the drain supply via the conducting transistors Q1 and Q2. When either or both of the inputs are logic 1 (voltage high), one or both of the upper transistors (Q1 and/or Q2) is off. One or both of the lower transistors (Q3 and/or Q4) is on, connecting the output to ground via the conducting channel. The output is low (≈ 0 V, logic 0). For the NAND gate, a logic 0 (low voltage) on one or both inputs causes one or both upper transistors (Q1 and/or Q2) to conduct, connecting the output to the drain supply voltage. The output is high ($\approx + V_{DD}$, logic 1). If both of the inputs are logic 1 (high voltage), the lower series transistors, Q3 and Q4, turn on and connect the output to ground. The output is low (≈ 0 V, logic 0).

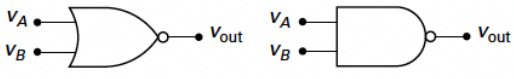
CMOS logic requires only a single supply voltage and is relatively easy to fabricate. The only input current that flows is that required to charge the gate-channel capacitances and any leakage through the off transistor. The power supply consumption is extremely low. Because of the low power consumption, the fan-out is very high. Speeds are comparable to that for ECL (see Table 2). Consequently, CMOS has the best overall properties of any logic family.



(a) basic gate: NOR



(b) basic gate: NAND



(c) logic symbol

v_A	v_B	v_{out}
L	L	H
L	H	L
H	L	L
H	H	L

NOR

v_A	v_B	v_{out}
L	L	H
L	H	H
H	L	H
H	H	L

NAND

(d) voltage truth tables

Figure 16: CMOS Logic

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PART V: MULTIVIBRATOR TYPES

Multivibrators

Multivibrators are pulse generator circuits that produce rectangular-wave outputs. There are three types.

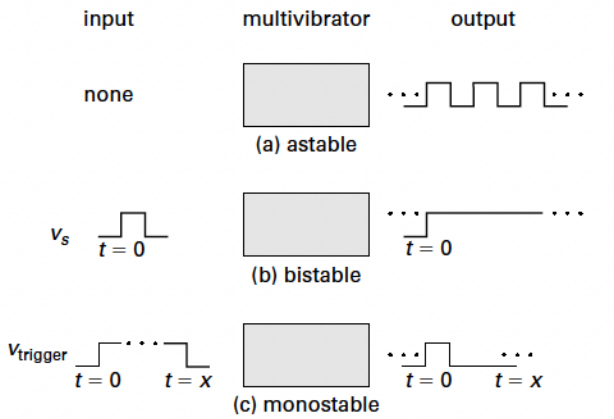

Figure 17: Multivibrator Types

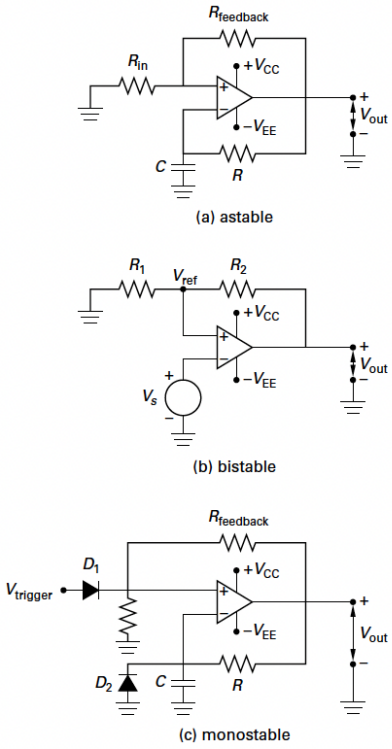

Figure 18: Multivibrator (Op Amp) Circuits

The *astable multivibrator*, also called the free-running multivibrator, has no particular stable state and generates a continuous flow of pulses without input, as shown in Fig. 33(a). The astable multivibrator may be used as a computer or digital system clock. The operational amplifier circuitry realization of an astable multivibrator is shown in Fig. 34(a).

The *bistable multivibrator* has two stable states and generates either a LOW or HIGH output as shown in Fig. 33(b). The bistable multivibrator is also called a *flip-flop*, and is used as a logic device. The operational amplifier circuitry realization of a bistable multivibrator is shown in Fig. 34(b).

The *monostable multivibrator* has a single stable state as shown in Fig. 33(c). The monostable multivibrator is also called a one-shot multivibrator and is used to generate a single pulse of known duration. This occurs because the duration of input pulse is unrelated to the duration of the output pulse, which is set by the circuitry. The operational amplifier circuitry realization of a monostable multivibrator is shown in Fig. 34(c). An important variation on the operational amplifier realization of these various vibrators uses an integrated circuit, which includes a bipolar or CMOS transistor. This widely used integrated circuit is the IC 555 timer (or one of its many variants manufactured by numerous companies), which can be connected to form all three types of multivibrators. Figure 35 shows the external connections, while Fig. 36 shows the internal circuitry. The proper connections to realize the astable, bistable, and monostable versions are shown in Fig. 37, Fig. 38, and Fig. 39.[14]

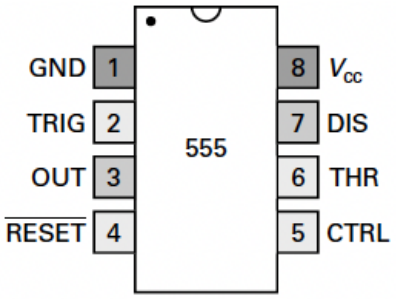

Figure 19: 555 Eight Pin Timer

[14] Excellent explanations of the internals and operations of this and many integrated circuits can be found online and also on the data sheets of the numerous companies that manufacture versions of the IC 555 Timer. For the licensed PE, knowing the basic operation and the expected output of this timer will allow for the proper connections.

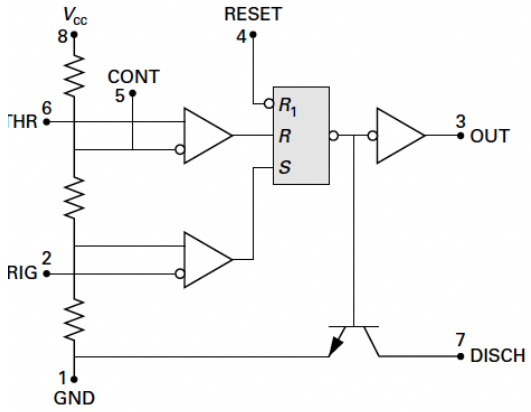

Figure 20: 555 Timer Astable Multivibrator Internal Block Diagram

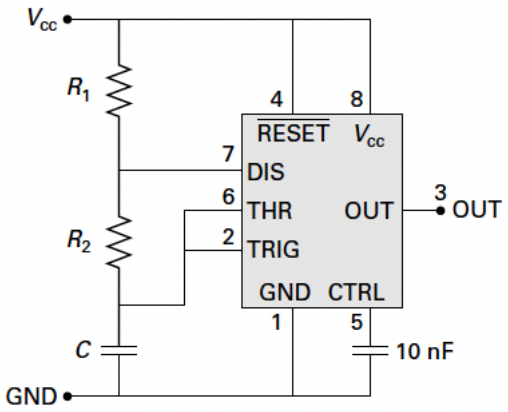

Figure 21: 555 Timer Astable Multivibrator Connections

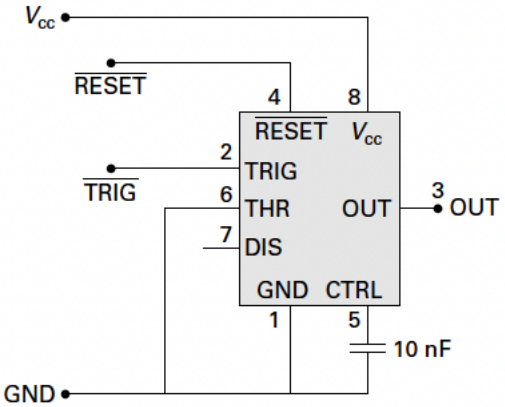

Figure 22: 555 Timer Bistable Multivibrator Connections

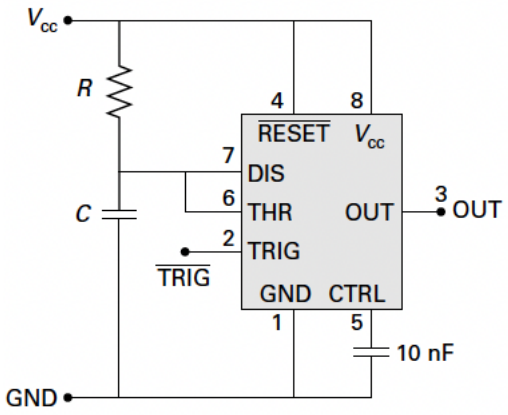

Figure 23: 555 Timer Monostable Multivibrator

PART VI: CIRCUITS AND DEVICES[15]

Circuit: Phase-Locked Loop (PLL)

A *phase-locked loop* (PLL) is a closed-loop control circuit for providing and outputting frequency that is exactly in phase with an incoming frequency.[16] A basic PLL is shown in Fig. 40. The circuit consists of a phase detector and a phase frequency detector, a loop (low-pass) filter, a voltage-controlled oscillator (VCO), and a feedback path. Both digital and analog PLLs have in common the phase detector, the VCO, and the feedback path.[17]

The phase detector compares the input frequency with the feedback frequency and outputs an error (or corrective) signal to the oscillator (via the loop filter) that then responds to drive the phase

[15] While some electronic devices are built from an array of individual components brought together on a printed circuit board (PCB), many can be purchased as single units with all functions included. Such devices are called *standard modular devices.*

[16] A mechanical analogy is tuning a piano. A tuning fork is used to provide a reference frequency. The piano string is adjusted until the beat frequency is inaudible. Another example is the manual transmission in an automobile. When being shifted, gears on the engine side and wheel side are turning at different rates. The rates must be matched before the shift is completed or a grinding sound is heard.

[17] The components considered to be part of an analog or digital PLL varies among texts. An analog PLL implements the phase detector, loop filter, and feedback function blocks with hardware components, while a digital PLL uses computed operations on binary words accomplished with either hardware or software digital signal processing (DSP). Also, an analog PLL uses a (VCO), while a digital PLL uses a numerically controlled oscillator (NCO), which is also called a digitally controlled oscillator (DCO). Even when transistors within a PLL operate between saturation and cutoff, this is not always considered digital operation. Practically, the function of the components, not their classification, is most important to the engineer.

difference between the two inputs to zero. An example is an exclusive OR gate or a more complex state machine called a *phase frequency detector* that compares zero crossing points. Both such detectors are digital. Both use the low-pass filter to smooth the output.

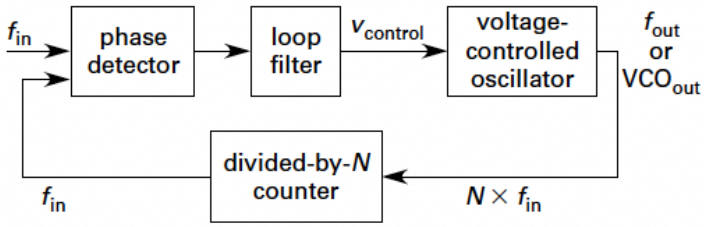

Figure 24: Phase-Locked Loop Functional Block Diagram

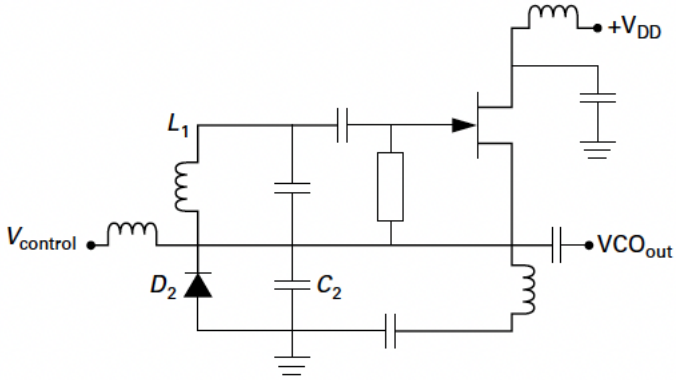

Figure 25: Voltage-Controlled Oscillator (VCO) Circuit

An example analog phase detector is the *four-quadrant multiplier* or *balance mixer* that multiplies the input reference signal with the oscillator feedback signal and generates a low-frequency signal with amplitude proportional to the phase difference (also called the *phase error*) between the input and the oscillator. The mixer also generates a higher frequency signal at twice the oscillator frequency, but this is eliminated by the lowpass filter.

The *voltage-controlled oscillator* uses the filter output and the controlling voltage input to generate an output frequency that is a multiple of the input frequency. Once fed back through the divide-by-*N* circuitry, the result drives the phase detector and filter to change the VCO voltage input until the frequencies are aligned at the output.

A digital VCO may consist of a clock source (crystal oscillator or multivibrator circuit), two counters, and a digital comparator. An analog VCO is shown in Fig. 41. The VCO uses the LRC *tank circuit* or *antiresonant circuit* that sets the frequency of the oscillator circuit.

Devices: RTDs and Resistant Bridges

A *resistance temperature device* (RTD), also known as a resistance temperature detector, is a sensor that uses changes in a material's electrical resistance to determine temperature. A r*esistance bridge* is used to measure the unknown output of an RTD. Resistance bridges can use two wires, three wires, or four wires. A two-wire bridge is used when a single element of the bridge varies; for example, when the RTD is the varying element. (See Fig. 42.) A three-wire bridge is used when a remotely located RTD (or thermistor) could experience lead resistance and noise pickup. (See Fig. 43.) A four-wire bridge provides additional accuracy and compensation for lead resistance issues, although normally these improvements are not worth the additional cost. Using operational amplifiers in conjunction with these bridges results in higher output levels and improved power dissipation, while minimizing output noise, distortion, and clipping. The bridge is in balance when the voltage at the output is zero, that is, when no current flows in an indicating device attached to the output terminals. When balanced, the relationship between the resistances is as follows.

Equation 12: RTD Balanced

$$\frac{R_{L1} + R_{\text{RTD}} + R_{L2}}{R_3} = \frac{R_2}{R_4}$$

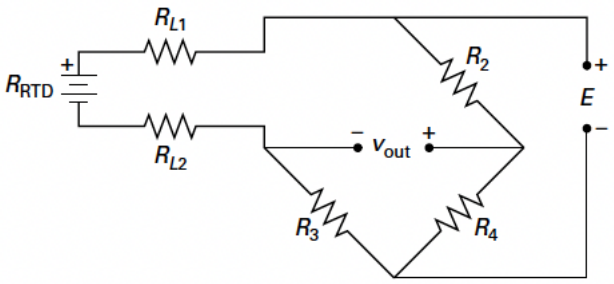

Figure 26: Two-Wire Resistance Bridge

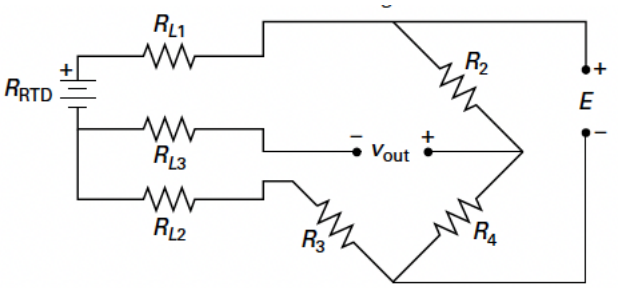

Figure 27: Three-Wire Resistance Bridge

The power supply and bridge resistances are normally located within control circuitry that can be tens or hundreds of feet from the RTD. Wire resistances can be significant, and temperature-driven resistance changes in the two wires further degrade accurate detection of temperature changes. The result is that the bridge has a nonzero output voltage, which causes an imbalance in the bridge. If the imbalance is small, it can be subtracted electronically from the output signal and the correct result obtained. If a large imbalance exists, the measurement range of the RTD (or other connected instrument) may be compromised.

The three-wire bridge shown in Fig. 43 is symmetrical along a line that runs through the bridge output corners. The negative of the output moves electronically from the top of R3 to the bottom of the RTD. Two lead wires, R_{L1} and R_{L2}, are on opposite arms of the bridge circuit. If the two wires are the same type and length, their resistances are equal and the bridge is in balance. Assuming both wires are run together, temperature changes in both wires will not unbalance the bridge because the effects are balanced in each wire. R_{L3} is a voltage-sensing wire and it provides the input signal at v_{out}. It carries a small current (in the microampere range in many cases) and is not in series with either bridge arm. It has no impact on the balance of the bridge circuit.

Example 3

A three-wire bridge with equal wire lengths leads to a sensor. How does the system remain balanced regardless of the lead resistance value?

Solution

Simplify the resistance relationship. From Fig. 43, the balanced (or null) relationship is

$$\frac{R_{L1}+R_{\mathrm{RTD}}}{R_{L2}+R_3}=\frac{R_2}{R_4}$$

$$\frac{R_{L1}\left(1+\dfrac{R_{\mathrm{RTD}}}{R_{L1}}\right)}{R_{L2}\left(1+\dfrac{R_3}{R_{L2}}\right)}=\frac{R_2}{R_4}$$

Since $R_{L1} = R_{L2}$, the values cancel. The resistance of each is known as R.

$$\frac{1+\dfrac{R_{\mathrm{RTD}}}{R}}{1+\dfrac{R_3}{R}}=\frac{R_2}{R_4}$$

The numerator and denominator on the left-hand side of the equation represent new resistance values, R'_{RTD} and R'_3 .

$$\frac{R'_{\mathrm{RTD}}}{R'_3}=\frac{R_2}{R_4}$$

Any changes in the value of R affect the numerator and denominator ratios equally. Only the change in resistance from the RTD impacts the balance.

Ladder Logic

Ladder logic is a rule-based programming language used primarily in *programmable logic controllers* (PLCs).[18] Ladder logic programs are useful where sequential control of a process is needed to ensure proper operation or protection of a power generation system. They are based on circuit diagrams and consist of horizontal lines arranged like the rungs of a ladder, each representing a *rule* that the engineer wants followed.

[18] PLC is a generic name for the original MODICON or modular digital controller that was the predecessor. The PLCs allow electromagnetic relays to be replaced by a digital computer running ladder logic using input lines from the appropriate sensors, meters, or gauges controlling electrical equipment.

Examples of ladder logic programs are shown in Fig. 44 and Fig. 45. The two vertical lines on the left and right side of the ladder are called *rails* and are connected to the power supply (usually, but not always, an AC voltage of 120 V). The left rail is the hot rail and is designated as L1, while the right rail is the neutral rail and is designated as L2 (see Fig. 44). Each line connecting the left and right rails is called a *rung*, which can consist of a number of different components, such as sensors, contacts, relays, timers, or any of the many electrical devices utilized in controlling equipment—all of which use standard electrical symbols.

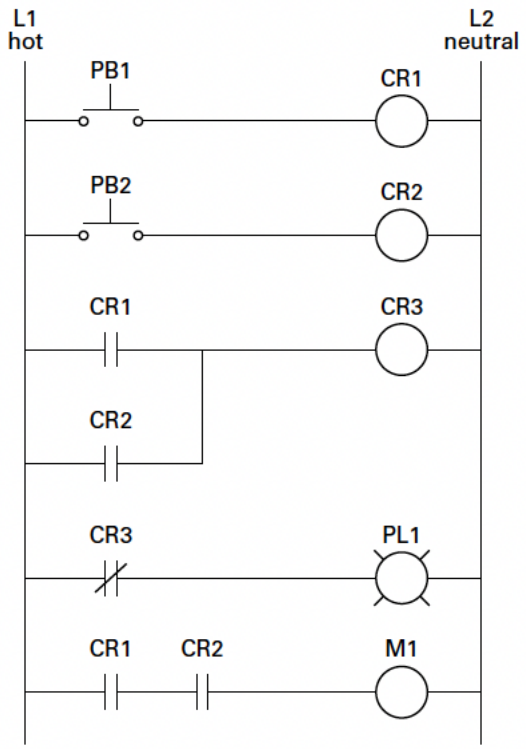

Figure 28: Ladder Logic with Standard Symbols

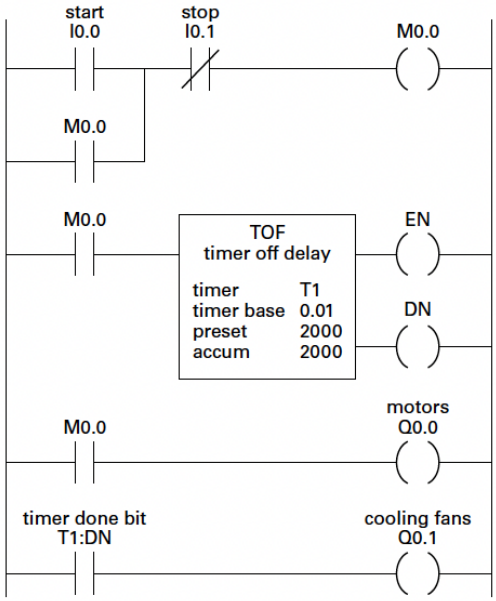

Figure 29: Ladder Logic with Timer

There are some exceptions to the standard symbols. For example, *contacts* may be indicated by regular brackets or inverse brackets (see Fig. 46), both of which have the same meaning. Also, relays and lights may be shown as partial circles rather than full circles.

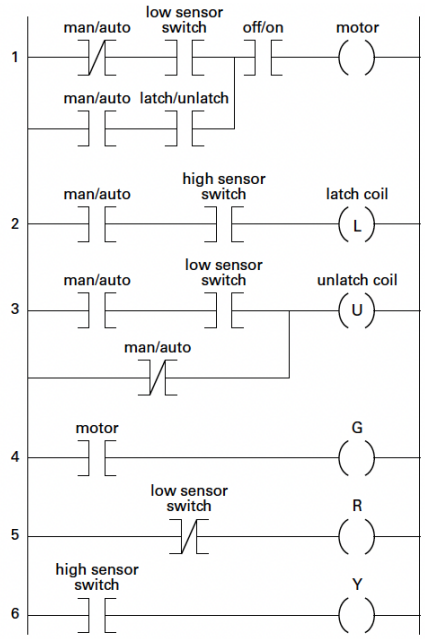

Figure 30: Ladder Logic with Nonstandard Symbols and Numbered Rungs

The normal condition of a contact (or a checker) on a rung is indicated by the presence or absence of a line connecting the brackets or parentheses. If no line is shown connecting the brackets, then the contact is normally open when the controlling *relay* is energized. If a line is shown, then the contact is normally closed when the controlling relay is energized. Ladder logic diagrams for standard logic gates are shown in Fig. 47.

The logic or rules in a ladder logic program are generally simple to discern and use common engineering symbols. Even so, the overall logic can be designed to control very complex systems. Originally, graphical ladder logic was limited to PLC programming, which was invented to control electromagnetic relay racks.[19] Since the programming may move faster than the physical relays, the timing differences must be accounted for in the logic, either through sequential control or delays. Depending upon the scan time of the PLC through a given portion of the logic, the implementation can seem to occur simultaneously. Understanding the interactions of the rungs with one another and the scan (timing) of the PLC are critical to proper programming.

[19] Such logic now exists in an assembly language format for more complex applications. The assembly language-like format is called Instruction List and can be found in IEC 61131-3.

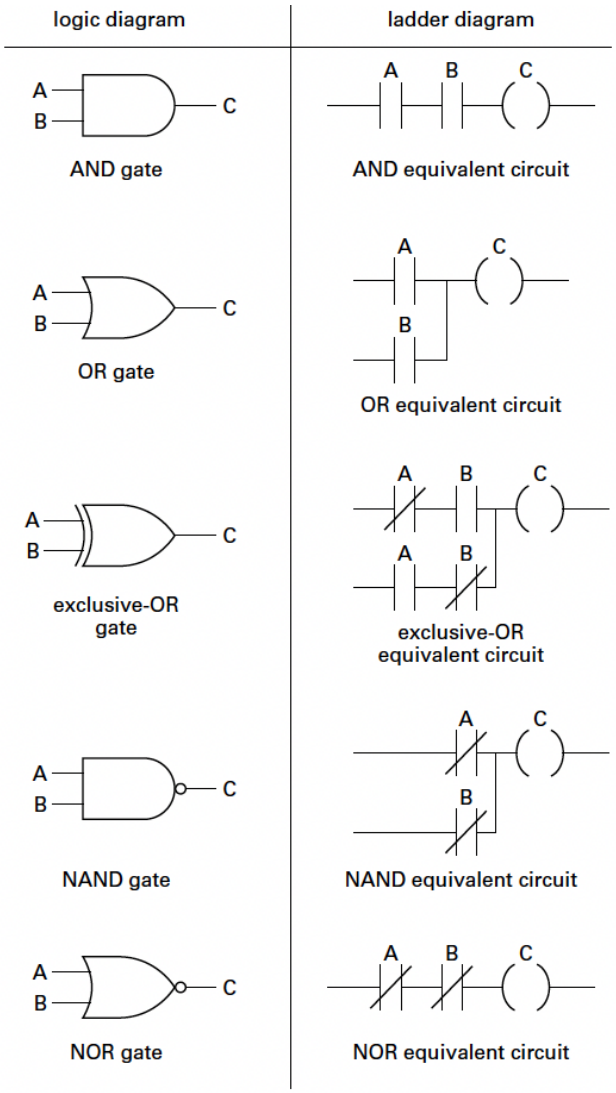

Figure 31: Ladder Logic for Standard Logic Gates

The logic or rules in a ladder logic program are generally simple to discern and use common engineering symbols. Even so, the overall logic can be designed to control very complex systems. Originally, graphical ladder logic was limited to PLC programming, which was invented to control electromagnetic relay racks.[20] Since the programming may move faster than the physical relays, the timing differences must be accounted for in the logic, either through sequential control or delays. Depending upon the scan time of the PLC through a given portion of the logic, the

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implementation can seem to occur simultaneously. Understanding the interactions of the rungs with one another and the scan (timing) of the PLC are critical to proper programming.

Logic checkers can be thought of as the contacts of a relay. The checkers control the voltage and provide the connection to the actuators, which can be thought of as a relay coil. The logic is read from the left side of the rung (the input) to the right side (output or load). If a complete path exists from left to right, the logic is considered true, or logic level 1. If no path exists, the logic is false, or logic level 0.

The ladder logic itself is the program coding designed to replace the electromagnetic relays in a normal control circuit. Some of the hardwired control circuits will remain and not be replaced by the ladder logic located in a digital computer. For example, emergency stop buttons are needed so the system can be disabled independent of a computer. The inputs that would have gone to a hardwired circuit provide the input to the ladder. Outputs that would have powered relays provide control signals to the output relays necessary to operate the equipment. An example showing common inputs (with the input addresses in boxes) on the left, the ladder logic corresponding to previously hardwired circuits in the middle, and the output to controlling relays (with output addresses in the diamond shapes) shown on the right is given in Fig. 48. The relays in the program coding section of the figure no longer physically exist.

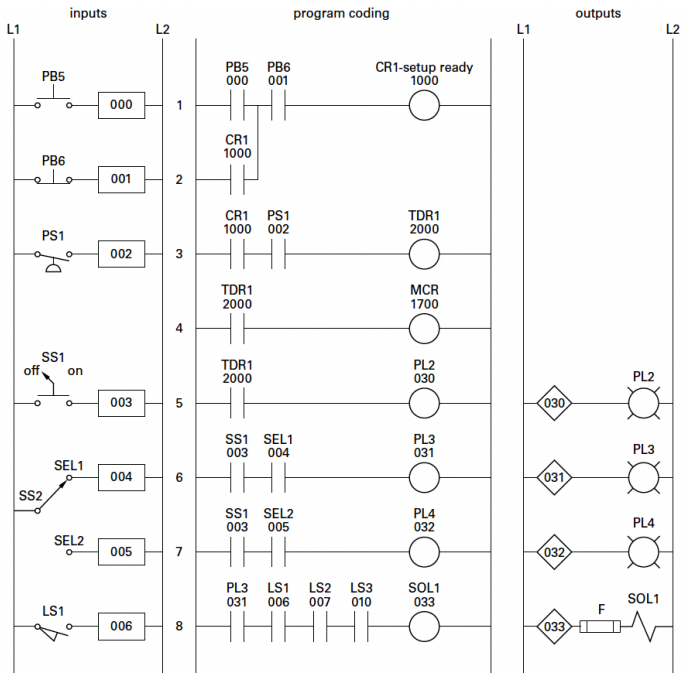

Figure 32: PLC and Ladder Logic Relationships

Example 4

What is the rule for rung 3 of the ladder logic in Fig. 44?

Solution

Since contacts CR1 and CR2 are in parallel, if either are closed, relay CR3 will turn on.

Ladder Logic Timers

Delays in the application of a rule, or logic on a given rung, are controlled by a timer. There are three basic types of timers.

The first type is an *on delay timer*, which uses the symbol TON. When the on delay timer has an input (i.e., a signal or voltage from the left side of the rung), the timer starts to count down. When a *preset time* is reached, the output of the delay timer turns on.[21] If the input signal is turned off before the countdown completes, the timer resets. See Fig. 49, which shows timer T1 with its input line off, as deduced from the accumulator number at 0 (i.e., the timer is designed to count down when the input line goes high).[22] It does so in 1 msec intervals per the *timer base* until it counts 1000 times, as given by the preset value. When the accumulator reaches 1000, the enable line goes high, or turns on. Since the accumulator only shows 0, no input signal has yet been received.

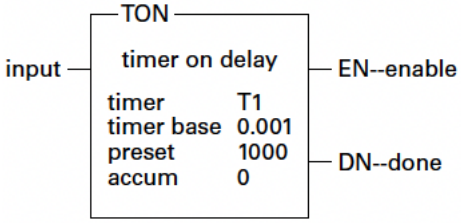

Figure 33: ON Delay Timer

[21] The terminology varies widely. “Turns on” means a signal is present on the line; the output is high; the logic level for that portion of the rung becomes 1; or simply a voltage now exists on the output.

[22] The timer input, shown as T1 in the figure, actually points toward a file that contains the timer model; therefore, on a ladder logic schematic, it might be shown as File Name:1. Manufacturers of PLCs often have tutorials on ladder logic and provide more in-depth information on any peculiarities specific to that manufacturer. Additionally, examples of timers and many other electrical devices can be found on YouTube®, which is useful as a quick reference.

The second type of timer is an *off delay timer*, which uses the symbol TOF, and is identical in operation to the on delay timer with the exception that the countdown begins when the input line is off. If the input signal is turned on before the countdown is complete, the timer resets. See Fig. 50 for an example that shows such a timer with the input line off and the done line, DN, high or on. The accumulator line shows a value of 1000, which matches the preset line, indicating the countdown is complete.

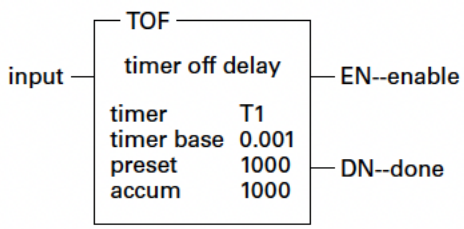

Figure 34: OFF Delay Timer

The third type of timer is called a retentive timer, which uses the symbol RTO. When the input line is on, the timer begins to count. The crucial difference between an RTO and a TON timer is that when the input line is turned off before the countdown completes, the count pauses (i.e., the accumulator count remains wherever it stops rather than resetting to zero).

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Items (latest editions) in **bold** are highly recommended for in-depth study.

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B. Camara, John A. *PE Power Reference Manual*. Belmont, CA: PPI (Kaplan), 2021.

C. Marne, David J., and John A. Palmer. *National Electrical Safety Code®* (NESC®) *2023 Handbook*. New York: McGraw Hill, 2023.

D. Earley, Mark, ed. *NFPA 70, National Electrical Code Handbook*. Quincy, Massachusetts: NFPA, 2020.

NOTE

Electrical refers to something related to electricity while "electric" refers to a device or machine that runs on electricity. Nevertheless, the NEC is sometimes referred to as the National Electric Code.

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Appendix A: Equivalent Units Of Derived And Common SI Units

Symbol	Equivalent Units			
A	C/s	W/V	V/Ω	J/(s·V)
C	A·s	J/V	(N·m)/V	V·F
F	C/V	C^2/J	s/Ω	(A·s)/V
F/m	C/(V·m)	C^2/(J·m)	C^2/(N·m^2)	s/(Ω·m)
H	W/A	(V·s)/A	Ω·s	(T·m^2)/A
Hz	1/s	s^{-1}	cycles/s	radians/(2π·s)
J	N·m	V·C	W·s	(kg·m^2)/s^2
m^2/s^2	J/kg	(N·m)/kg	(V·C)/kg	(C·m^2)/($A·s^3$)
N	J/m	(V·C)/m	(W·C)/(A·m)	(kg·m)/s^2
N/A^2	Wb/(N·m^2)	(V·s)/(N·m^2)	T/N	1/(A·m)
Pa	N/m^2	J/m^3	(W·s)/m^3	kg/(m·s^2)
Ω	V/A	W/A^2	V^2/W	(kg·m^2)/($A^2·s^3$)
S	A/V	1/Ω	A^2/W	($A^2·s^3$)/(kg·m^2)
T	Wb/m^2	N/(A·m)	(N·s)/(C·m)	kg/(A·s^2)
V	J/C	W/A	C/F	(kg·m^2)/($A·s^3$)
V/m	N/C	W/(A·m)	J/(A·m·s)	(kg·m)/($A·s^3$)
W	J/s	V·A	V^2 / Ω	(kg·m^2)/s^3
Wb	V·s	H·A	T/m^2	(kg·m^2)/($A·s^2$)

Appendix B: Physical Constants

Table Note 1

Quantity	Symbol	US Customary	SI Units
Charge			
electron	e		-1.6022×10^{-19} C
proton	p		$+1.6022 \times 10^{-19}$ C
Density			
air [STP][32°F, (0°C)]		0.0805 lbm/ft^3	1.29 kg/m^3
air [70°F, (20°C), 1 atm]		0.0749 lbm/ft^3	1.20 kg/m^3
sea water		64 lbm/ft^3	1025 kg/m^3
water [mean]		62.4 lbm/ft^3	1000 kg/m^3
Distance			
Earth radius[2]	$\oplus$	2.09×10^{7} ft	6.370×10^{6} m
Earth-Moon separation[2]	$\oplus\leftmoon$	1.26×10^{9} ft	3.84×10^{8} m
Earth-Sun separtion[2]	$\oplus\odot$	4.89×10^{11} ft	1.49×10^{11} m
Moon radius[2]	$\leftmoon$	5.71×10^{6} ft	1.74×10^{6} m
Sun radius[2]	$\odot$	2.28×10^{9} ft	6.96×10^{8} m
first Bohr radius	a_0	1.736×10^{-10} ft	5.292×10^{-11} m
Gravitational Acceleration			
Earth [mean]	g	32.174 (32.2) ft/sec^2	9.8067 (9.81) m/s^2
Mass			
atomic mass unit	μ or m_μ $\frac{1}{12}m(^{12}C)$	3.66×10^{-27} lbm	1.6606×10^{-27} kg or 10^{-3} kg mol^{-1} / N_A or 931.481 MeV
Earth[2]	$\oplus$	4.11×10^{23} slugs	6.00×10^{24} kg
Earth [customary U.S.][2]	$\oplus$	1.32×10^{25} lbm	-
Moon[2]	$\leftmoon$	1.623×10^{23} lbm	7.36×10^{22} kg
Sun[2]	$\odot$	4.387×10^{30} lbm	1.99×10^{30} kg
electron rest mass	m_e	2.008×10^{-30} lbm	9.109×10^{-31} kg [0.511 MeV]
neutron rest mass	m_n	3.693×10^{-27} lbm	1.675×10^{-27} kg [939.6 MeV]
proton rest mass	m_p	3.688×10^{-27} lbm	1.672×10^{-27} kg [938.2 MeV]
Pressure			

Quantity	Symbol	US Customary	SI Units
atmospheric		14.696 (14.7) lbf/in^2	1.0133□10^5 Pa
Temperature			
standard		32°F (492°R)	0°C (273 K)
absolute zero		–459.67°F (0°R)	–273.16°C (0 K)
Velocity[3]			
Earth escape		3.67□10^4 ft/sec	1.12□10^4 m/s
light (vacuum)	*c*, c_0	9.84□10^8 ft/sec	2.9979 (3.00) □10^8 m/s
sound [air, STP]	*a*	1090 ft/sec	331 m/s
sound [air, 70°F, (20°C), 1 atm]		1130 ft/sec	344 ft/s
Volume			
Volume: molal ideal gas (STP)[4]		359 ft^3 / lbmol	22.41 m^3/kmol

Table 1 Notes

1. Units come from a variety of sources, but primarily from the Handbook of Chemistry and Physics, The Standard Handbook for Aeronautical and Astronautical Engineers, and the Electrical Engineering Reference Manual for the PE Exam. See also the NIST website at https://pml.nist.gov/cuu/Constants/.
2. Symbols shown for the solar system are those used by NASA. See https://science.nasa.gov/resource/solar-system-symbols/.
3. Velocity technically is a vector. It has direction.
4. The unit “lbmol” is an actual unit, not a misspelling.

Appendix C: Fundamental Constants

Quantity	Symbols	US Customary	SI Units
Avogadro's number	N_A, L		6.022×10^{23} mol^{-1}
Bohr magneton	$\propto_B$		9.2732×10^{-24} J/T
Boltzmann constant	κ	5.65×10^{-24} ft-lbf/ R	1.3805×10^{-23} J/T
electron volt: $\left(\frac{e}{C}\right)$ J	eV		1.602×10^{-19} J
Faraday constant, $N_A e$	F		96485 C/mol
fine structure constant, inverse α^{-1}	α α^{-1}		7.297×10^{-3} ($\approx$1/137) 137.035
gravitational constant	g_c	32.174 lbm-ft/lbf-sec^2	
Newtonian gravitational constant	G	3.44×10^{-8} ft^4 / lbf-sec^4	6.672×10^{-11} N×m^2 / kg^2
nuclear magneton	$\propto_N$		5.050×10^{-27} J/T
permeability of a vacuum	$\propto_0$		1.2566×10^{-6} N/A^2 (H/m)
permittivity of a vacuum, electric constant $1/\mu_0 c^2$	ε_0		8.854×10^{-12} C^2 / N×m^2 (F/m)
Planck's constant	h		6.6256×10^{-34} J×s
Planck's constant: h/2π			1.0546×10^{-34} J×s
Rydberg constant	R_∞		1.097×10^7 m^{-1}
specific gas constant, air	R	53.3 ft-lbf/lbm- R	287 J/kg×K
Stefan-Boltzmann constant		1.71×10^{-9} BTU/ft^2-hr-°R^4	5.670×10^{-8} W/m^2 ×K^4
triple point, water		32.02 F, 0.0888 psia	0.01109 C, 0.6123 kPa
universal gas constant	R*	1545 ft-lbf/lbmol- R 1.986 BTU/lbmol- R	8314 J/kmol×K

Table Notes

1. Units come from a variety of sources, but primarily from the Handbook of Chemistry and Physics, The Standard Handbook for Aeronautical and Astronautical Engineers, and the Electrical Engineering Reference Manual for the PE Exam. See also the NIST website at https://pml.nist.gov/cuu/Constants/. The unit in Volume of "lbmol" is an actual unit, not a misspelling.

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Appendix D: Mathematical Constants, Signs/Symbols, Maxwell's Equations

Quantity	Symbol	Value
Archimedes' constant (pi)	π	3.1415926536
base of natural logs	*e*	2.7182818285
Euler's constant	*C* or τ	0.5772156649

Signs/Symbols	Meaning
·	multiplied by
/	divided by
:	ratio
≫	much greater than
≪	much less than
=	equals
≡	identical with
~	similar to
≈	approximately equals
≅	approximately equals, congruent
→ , ≐	approaches
∝	proportional, varies as
∴	therefore

Maxwell's Equations

integral form	point form	remarks
$\oint_s \mathbf{D}\cdot d\mathbf{s} = \int_V \rho\, dv$	$\nabla\cdot\mathbf{D} = \rho$	Gauss' law
$\oint_s \mathbf{B}\cdot d\mathbf{s} = 0$	$\nabla\cdot\mathbf{B} = 0$	nonexistence of magnetic monopoles
$\oint \mathbf{E}\cdot d\mathbf{l} = \int_s \left(\frac{-\partial \mathbf{B}}{\partial t}\right)\cdot d\mathbf{s}$	$\nabla\times\mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$	Faraday's law
$\oint \mathbf{H}\cdot d\mathbf{l} = \int_s \left(\mathbf{J}_c + \frac{\partial \mathbf{D}}{\partial t}\right)\cdot d\mathbf{s}$	$\nabla\times\mathbf{H} = \mathbf{J}_c + \frac{\partial \mathbf{D}}{dt}$	Ampère's law

Free-Space Form

integral form	point form
$\oint_s \mathbf{D}\cdot d\mathbf{s} = 0$	$\nabla\cdot\mathbf{D} = 0$
$\oint_s \mathbf{B}\cdot d\mathbf{s} = 0$	$\nabla\cdot\mathbf{B} = 0$
$\oint \mathbf{E}\cdot d\mathbf{l} = \int_s \left(\frac{-\partial \mathbf{B}}{\partial t}\right)\cdot d\mathbf{s}$	$\nabla\times\mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$
$\oint \mathbf{H}\cdot d\mathbf{l} = \int_s \left(\frac{\partial \mathbf{D}}{\partial t}\right)\cdot d\mathbf{s}$	$\nabla\times\mathbf{H} = \frac{\partial \mathbf{D}}{dt}$

Electromagnetic Field Vector Equations

$$\mathbf{D} = \epsilon\mathbf{E} = \epsilon_0\mathbf{E} + \mathbf{P} = \epsilon_0(1+\chi_e)\mathbf{E}$$
$$\mathbf{B} = \mu\mathbf{H} = \mu_0\mathbf{H} + \mu_0\mathbf{M} = \mu_0(1+\chi_m)\mathbf{H}$$
$$\mathbf{J} = \sigma\mathbf{E} = \rho\mathbf{v}$$

Appendix E: The Greek Alphabet

A	α	alpha	N	υ	nu
B	β	beta	Ξ	ξ	xi
Γ	γ	gamma	O	o	omicron
Δ	δ	delta	Π	π	pi
E	ε	epsilon	P	ρ	rho
Z	ζ	zeta	Σ	σ	sigma
H	η	eta	T	τ	tau
Θ	θ	theta	ϒ	υ	upsilon
I	ι	iota	Φ	ϕ	phi
K	κ	kappa	X	χ	chi
Λ	λ	lambda	Ψ	ψ	psi
M	μ	mu	Ω	ω	omega

Appendix F: SI Prefixes

symbol	prefix	value
a	atto	10^{-18}
f	femto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
c	centi	10^{-2}
d	deci	10^{-1}
da	deka	10
h	hecto	10^{2}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}
P	peta	10^{15}
E	exa	10^{18}

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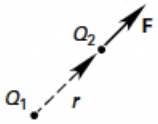
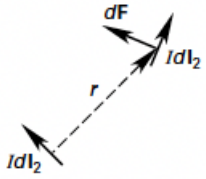
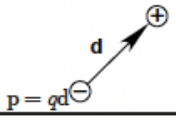
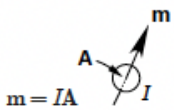
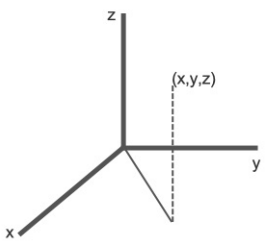
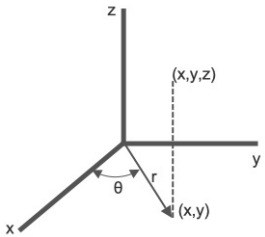
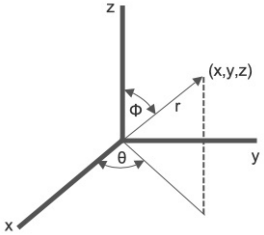
Appendix G: Comparison of Electric & Magnetic Equations

equation description	electric version	magnetic version	remarks
experimental force law	Coulomb's law $\mathbf{F} = \left(\frac{Q_1 Q_2}{4\pi\epsilon r^2}\right)\mathbf{r}$ 	force between two current elements $d\mathbf{F} = \left(\frac{\mu_0}{4\pi}\right)\left(\frac{I_2 d\mathbf{l}_2 \times (I_1 d\mathbf{l}_1 \times r)}{r^2}\right)$ 	The term $Id\mathbf{l}$ in the magnetic column is the equivalent of a "magnetic charge" q_m. The I or the $d\mathbf{l}$ can be the vector. The r is a unit vector pointing from 1 to 2.
field definitions from force law	$\mathbf{F} = Q\mathbf{E}$	$d\mathbf{F} = \mathbf{I}\times\mathbf{B}dl$ current element $d\mathbf{F} = \mathbf{J}\times\mathbf{B}dV$ distributed current element $d\mathbf{F} = q\mathbf{v}\times\mathbf{B}$ moving charge	The V used in this row represents volume, not voltage. The v is the velocity.
general force law	$\mathbf{F} = q(\mathbf{E} + \mathbf{v}\times\mathbf{B})$ $d\mathbf{F} = (\rho\mathbf{E} + \mathbf{J}\times\mathbf{B})dV$ where $dQ = \rho dV$		The V in this row represents the volume, not voltage. The v is the velocity.
definition of scalar and vector potential	$E = -\nabla V$	$\mathbf{B} = \nabla \times \mathbf{A}$	**A** is the magnetic vector potential.
Poisson's equation for the potential function	$\nabla^2 V = -\frac{\rho}{\epsilon}$	$\nabla^2 \mathbf{A} = -\mu_0 \mathbf{J}$	From a knowledge of the charge distribution, the potential can be found and then the **E** and **B** fields determined.
Gauss's law enclosing charge and Ampère's law enclosing current	$\iint \mathbf{D}\cdot d\mathbf{A} =$ $\iiint \rho dV = Q$ $\nabla\cdot\mathbf{D} = \rho$	$\oint H\cdot d\mathbf{l} = I$ $\nabla \times \mathbf{H} = \mathbf{J}$	The V in this row represents volume.
constitutive relations	$\mathbf{D} = \epsilon\mathbf{E}$ $\mathbf{D} = \epsilon_0\mathbf{E} + \mathbf{P}$	$\mathbf{B} = \mu\mathbf{H}$ $\mathbf{B} = \mu_0\mathbf{H} + \mu_0\mathbf{M}$	The second set of equations is always valid. The first set assumes the medium is linear and isotropic.
definitions of relative permittivity and permeability	$\epsilon_r = \frac{\epsilon}{\epsilon_0}$ $\epsilon_0 =$ 8.854×10^{-12} F/m	$\mu_r = \frac{\mu}{\mu_0}$ $\mu_0 = 4\pi \times 10^{-7}$ H/m	

equation description	electric version	magnetic version	remarks
capacitance and inductance of a field cell	$\epsilon_0 = \frac{C}{l}$	$\mu_0 = \frac{L}{l}$	Field cells are a construct designed to represent free space in terms of a parallel plate capacitor and an inductor. This capacitance and inductance exist regardless of the presence of an electric or magnetic field.
capacitance and inductance	$C = \frac{Q}{V}$	$L = \frac{\Lambda}{I}$	Λ is the flux linkage.
energy density of a field	$U = \frac{1}{2}\epsilon E^2$	$U = \frac{1}{2}\mu H^2$	Both energy and momentum are carried by a field.
energy stored by capacitance and inductance	$W = \frac{1}{2}CV^2$	$W = \frac{1}{2}LI^2$	
electromotive and magnetomotive force with sources present	$\oint \mathcal{E}\cdot d\mathbf{l} = \mathcal{E} = V$	$\oint \mathbf{H}\cdot d\mathbf{l} = NI = F_m = V_m$	The $\mathcal{E}$ is the emf, not the permittivity. Without sources present, both line integrals are equal to zero.
dipole moments			
dipole torque	$\mathbf{T} = \mathbf{p} \times \mathbf{E}$	$\mathbf{T} = \mathbf{m} \times \mathbf{B}$	This torque occurs due to the dipole being immersed in an external **E** or **B** field.
dipole potential energy	$W = -\mathbf{p}\cdot\mathbf{E}$	$W = -\mathbf{m}\cdot\mathbf{B}$	

electric	magnetic
emf $= V = IR$	mmf $= V_m = \phi\mathcal{R}$
current I	flux ϕ
emf $\mathcal{E}$ or V	mmf V_m
resistance $R = \rho l/A = l/\sigma A$	reluctance $\mathcal{R} = l/\mu A$
resistivity ρ	reluctivity $1/\mu$
conductance $G = 1/R$	permeance $P_m = \mu A/l$
conductivity $\sigma = 1/\rho$	permeability μ

Appendix H: Coordinate Systems and Related Operations

Mathematical Operations	Rectangular Coordinates	Cylindrical Coordinates	Spherical Coordinates
Conversion to Rectangular Coordinants	 $x = x$ $y = y$ $z = z$	 $x = r\cos\theta$ $y = r\sin\theta$ $z = z$	 $x = r\sin\phi\cos\theta$ $y = r\sin\phi\sin\theta$ $z = r\cos\phi$
Gradient	$\nabla f = \frac{\partial f}{\partial x}\mathbf{i} + \frac{\partial f}{\partial y}\mathbf{j} + \frac{\partial f}{\partial z}\mathbf{k}$	$\nabla f = \frac{\partial f}{\partial r}\mathbf{r} + \frac{1}{r}\frac{\partial f}{\partial \theta}\boldsymbol{\theta} + \frac{\partial f}{\partial z}\mathbf{k}$	$\nabla f = \frac{\partial f}{\partial r}\mathbf{r} + \frac{1}{r}\frac{\partial f}{\partial \phi}\boldsymbol{\phi} + \frac{1}{r\sin\theta}\frac{\partial f}{\partial \theta}\boldsymbol{\theta}$
Divergence	$\nabla \cdot \mathbf{A} = \frac{\partial A_x}{\partial x} + \frac{\partial A_y}{\partial y} + \frac{\partial A_z}{\partial z}$	$\nabla \cdot \mathbf{A} = \frac{1}{r}\frac{\partial (rA_r)}{\partial r} + \frac{1}{r}\frac{\partial A_\theta}{\partial \theta} + \frac{\partial A_z}{\partial z}$	$\nabla \cdot \mathbf{A} = \frac{1}{r^2}\frac{\partial (r^2 A_r)}{\partial r} + \frac{1}{r\sin\phi}\frac{\partial (A_\phi \sin\phi)}{\partial \phi} + \frac{1}{r\sin\phi}\frac{\partial A_\theta}{\partial \theta}$
Curl	$\nabla \times \mathbf{A} = \begin{vmatrix} \mathbf{i} & \mathbf{j} & \mathbf{k} \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \frac{\partial}{\partial z} \\ A_x & A_y & A_z \end{vmatrix}$	$\nabla \times \mathbf{A} = \begin{vmatrix} \frac{1}{r}\mathbf{r} & \boldsymbol{\theta} & \frac{1}{r}\mathbf{k} \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial \theta} & \frac{\partial}{\partial z} \\ A_r & A_\theta & A_z \end{vmatrix}$	$\nabla \times \mathbf{A} = \begin{vmatrix} \frac{1}{r^2\sin\theta}\mathbf{r} & \frac{1}{r^2\sin\theta}\boldsymbol{\phi} & \frac{1}{r}\boldsymbol{\theta} \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial \phi} & \frac{\partial}{\partial \theta} \\ A_r & rA_\phi & rA\theta A_\phi \end{vmatrix}$
Laplacian	$\nabla^2 f = \frac{\partial^2 f}{\partial x^2} + \frac{\partial^2 f}{\partial y^2} + \frac{\partial^2 f}{\partial z^2}$	$\nabla^2 f = \frac{1}{r}\frac{\partial r}{\partial r}\left(r\frac{\partial f}{\partial r}\right) + \frac{1}{r^2}\frac{\partial^2 f}{\partial \theta^2} + \frac{\partial^2 \phi}{\partial z^2}$	$\nabla^2 f = \frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial f}{\partial r}\right) + \frac{1}{r^2\sin\phi}\frac{\partial}{\partial \phi}\left(\sin\phi\frac{\partial f}{\partial \phi}\right) + \frac{1}{r^2\sin^2\phi}\left(\frac{\partial^2 f}{\partial \theta^2}\right)$

